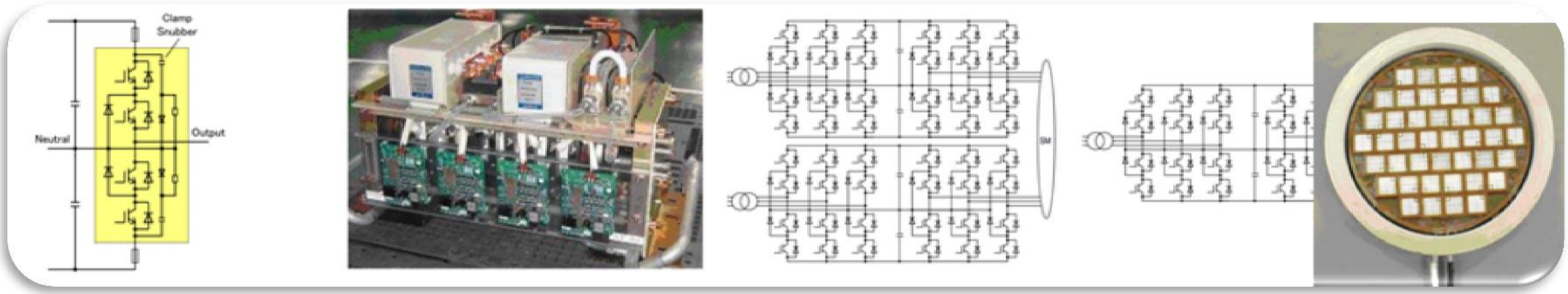


Power semiconductor device: Basics

Ichiro Omura
Kyushu Institute of Technology
Japan

IEEE EDS Webinar Dec. 2, 2015

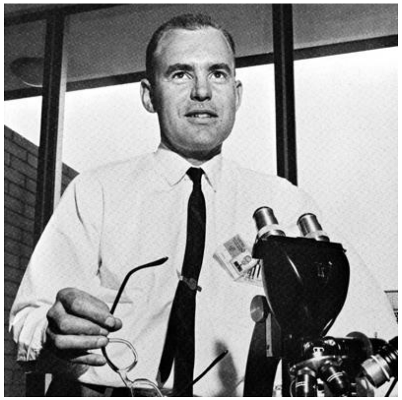
Outline

- Introduction
  - History
  - Power electronics circuit
- Power semiconductor devices
  - Power MOSFET / Super-junction MOSFET
  - IGBT
  - Thyristors
  - Lateral devices
- Future possibility
- Related technology

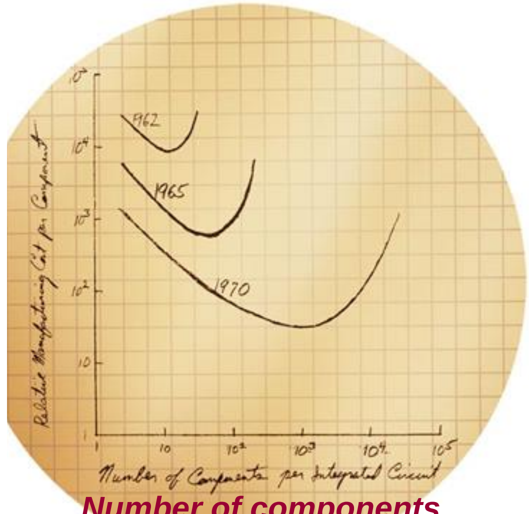
1965 - "Moore's Law"
Silicon Engine to drive ICT

COMPUTER HISTORY MUSEUM

Gordon E. Moore



Manufacturing cost per component



Number of components per integrated circuit

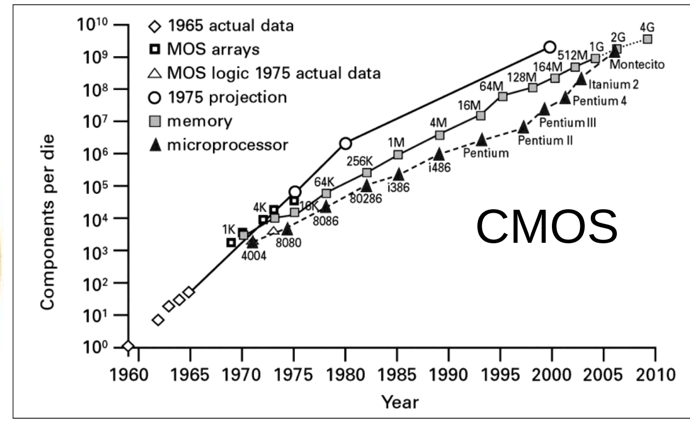
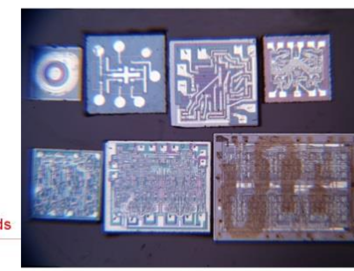
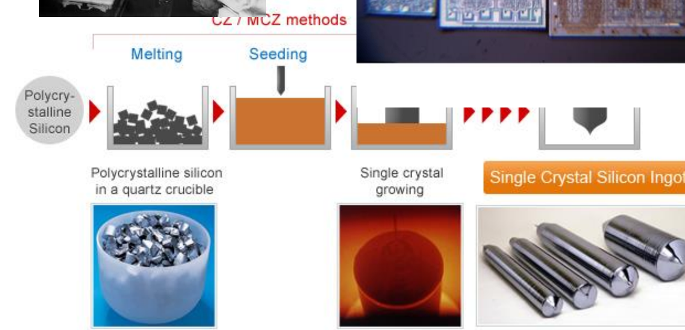


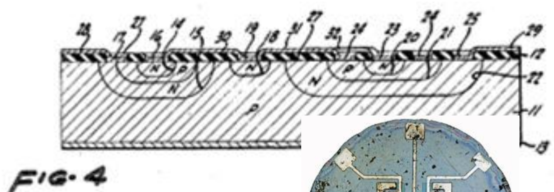
FIGURE 9. Integrated circuit complexity, actual data compared with 1975 projection. Source: Intel.

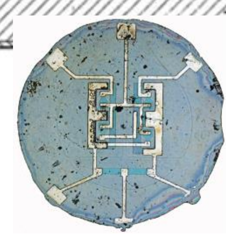




Robert Noyce

Integrated circuit patent in 1959





To digital cost free => ICT for everybody

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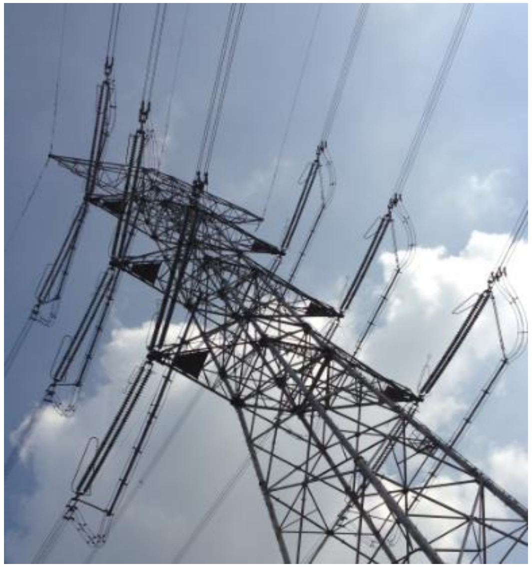
AC power distribution system

transm.web.fc2.com

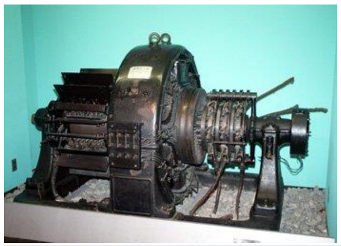


www.cz-toshiba.com

AC to AC
Constant frequency
No active control function

100 years of power device development (High voltage)

1940



Rotary converter
(AC-DC)

Electric Machine

mm

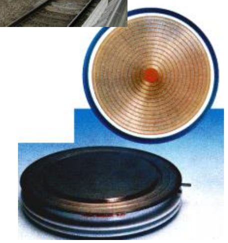
1960

Mercury arc rectifier
(AC-DC)

Electronics
(Vacum Tubes)

0.1mm

1980



Thyristor/GTO
(AC-DC/DC-AC)

R&D

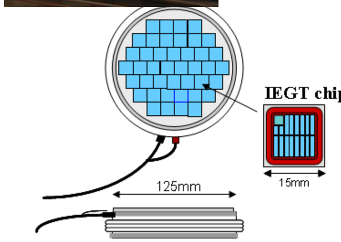
Neutron doped FZ wafer

Carrier lifetime control

Semiconductor
Technology

10-100um

2000



IGBT
(AC-DC/DC-AC, MOS gate)

R&D

Carrier Injection Enhancement

Edge termination technology

Chip Parallel operation

Cosmic ray SEU

Thin wafer technology

Advanced LSI Tech.
(CMOS, DRAM)

<1-10um

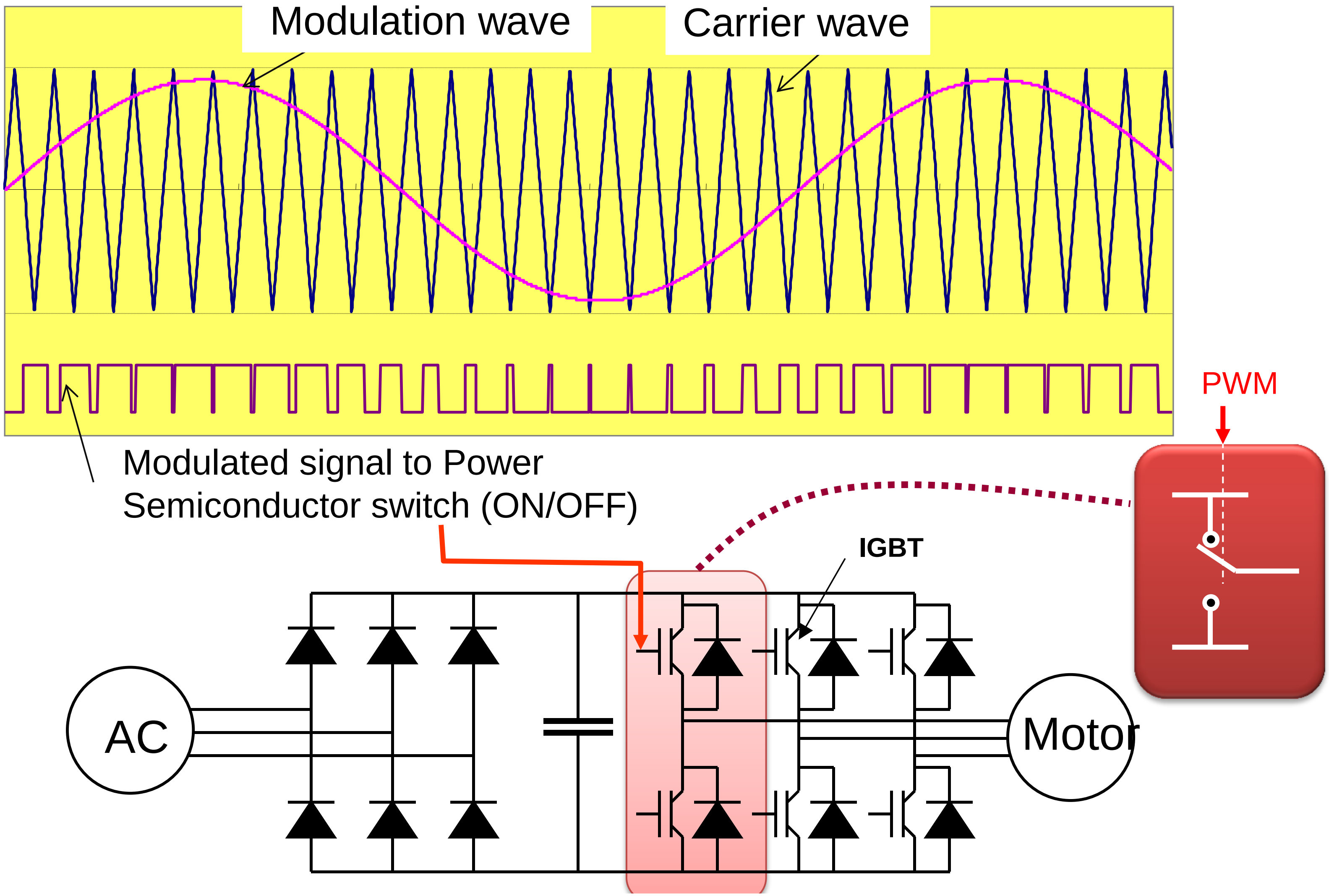
Manufacturing technology advancement

Photos:
Nippon inst. tech, Museum
Nikkei
Tokyu Museum
JR Kyushu
Nagahama Railway Museum
Toshiba

IGBT
Insulated Gate
Bipolar Transistor

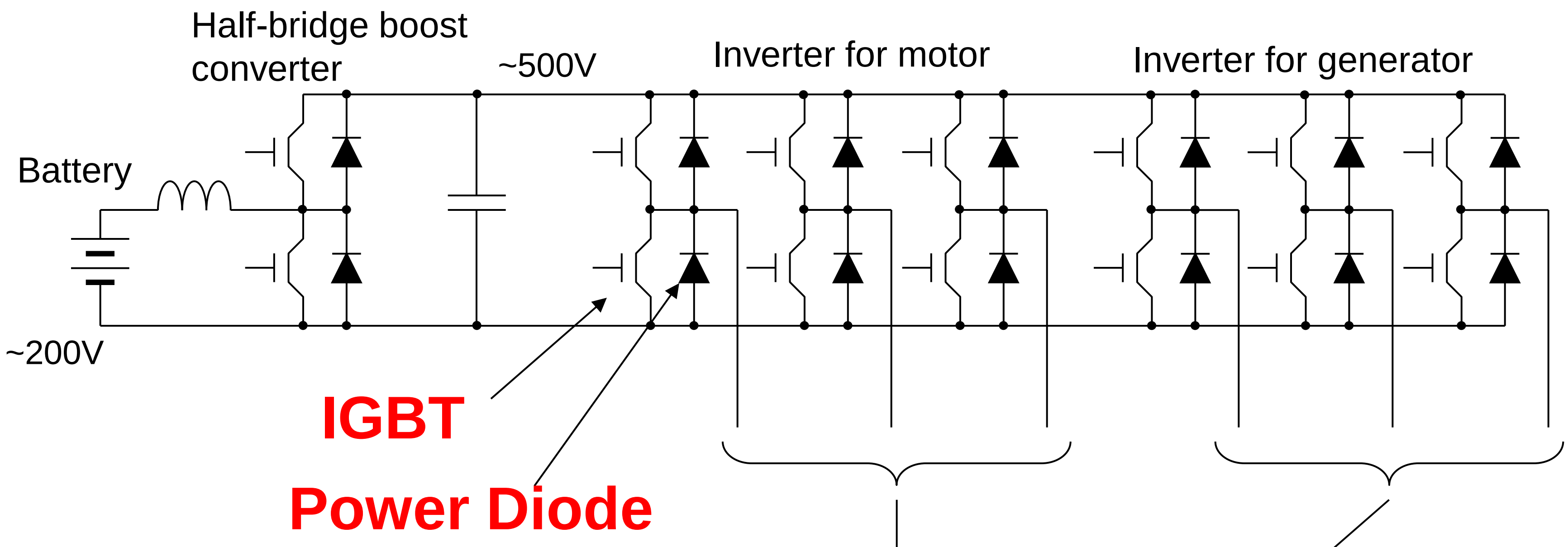
Ichiro Omura Kyushu Inst. Tech.

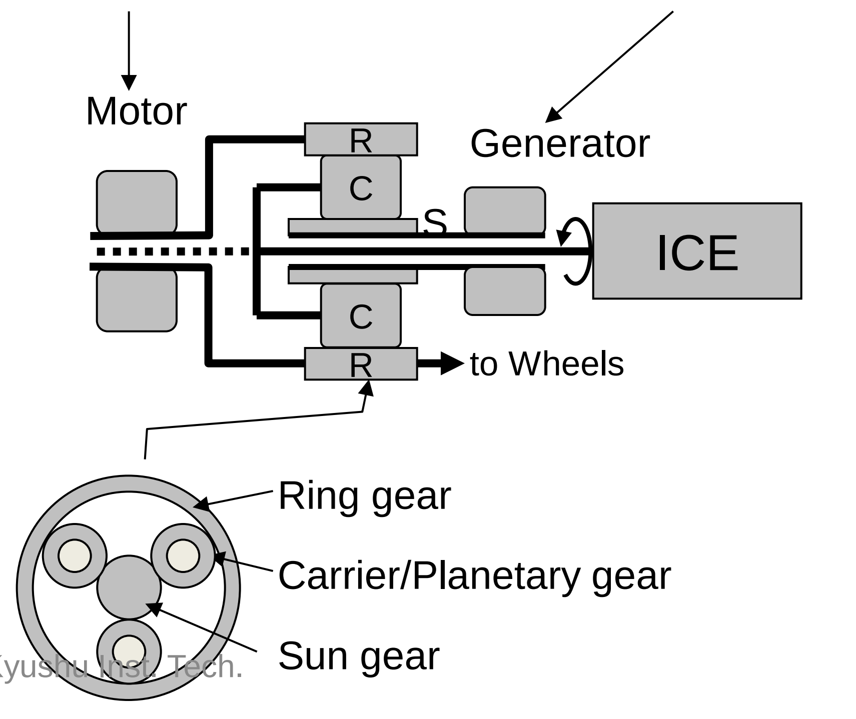
PWM: Pulse Width Modulation



1. PWM signal control power semiconductors switch (ON / OFF)
2. Motor current follows the modulation wave

Hybrid electric vehicle propulsion system





Total chip area for IGBT and power diode is more than **40 cm² of silicon wafer** for Toyota Prius[*].

Z. Shen and I. Omura. Proceeding of the IEEE, Vol. 95 No. 4, 2007.(Figure)
***A. Kawahashi et al., Proc. of ISPSD 2004, pp. 23-29, 2004.**

Power Semiconductor Devices

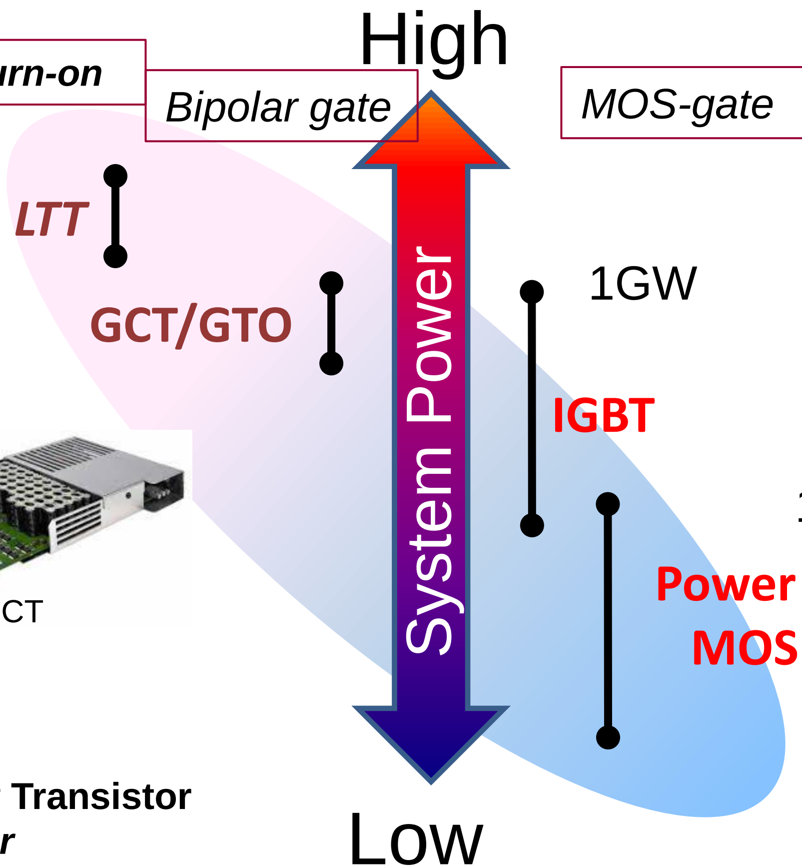
Power Semiconductor Devices

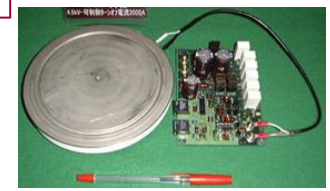
Vertical device

LTT

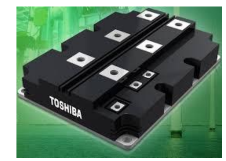
GTO

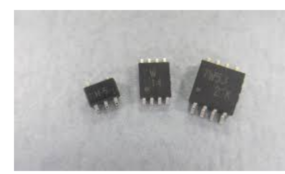
GCT





IGBT





Power MOS

IGBT: Insulated Gate Bipolar **Transistor**
GTO: Gate Turn-off ***Thyristor***
GCT: Gate Commutated Turn-off ***Thyristor***
LTT: Light Triggered ***Thyrisotor*** (optical fiber coupled)

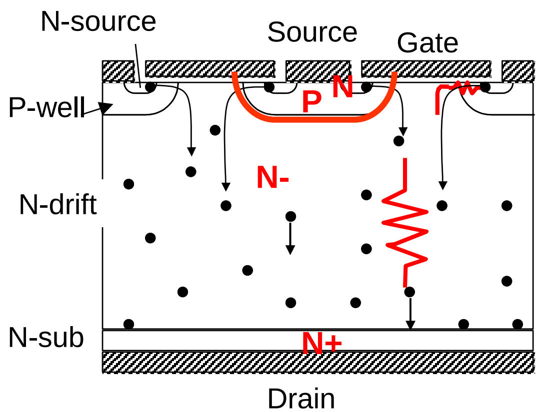
- **MOS gate devices cover wide-power range.**
- **Bipolar gate devices cover very high power applications(>10MW).**

Photos:
Infineon
Toshiba
ABB
TMEIC

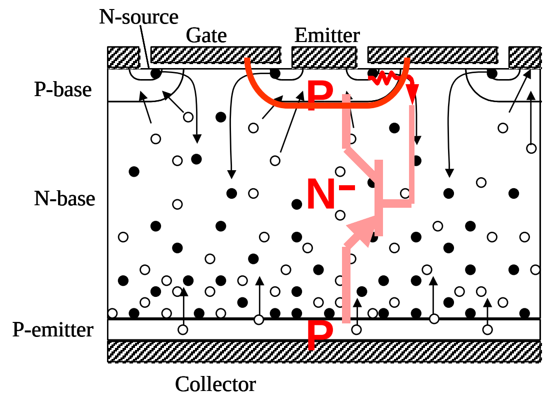
Types of power semiconductors(Switch)

MOS control + Unipolar

Power MOSFET

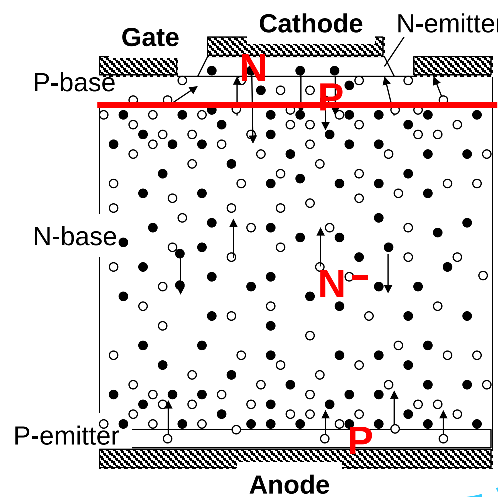


IGBT



MOS control + Bipolar

Thyristors (GTO,GCT)

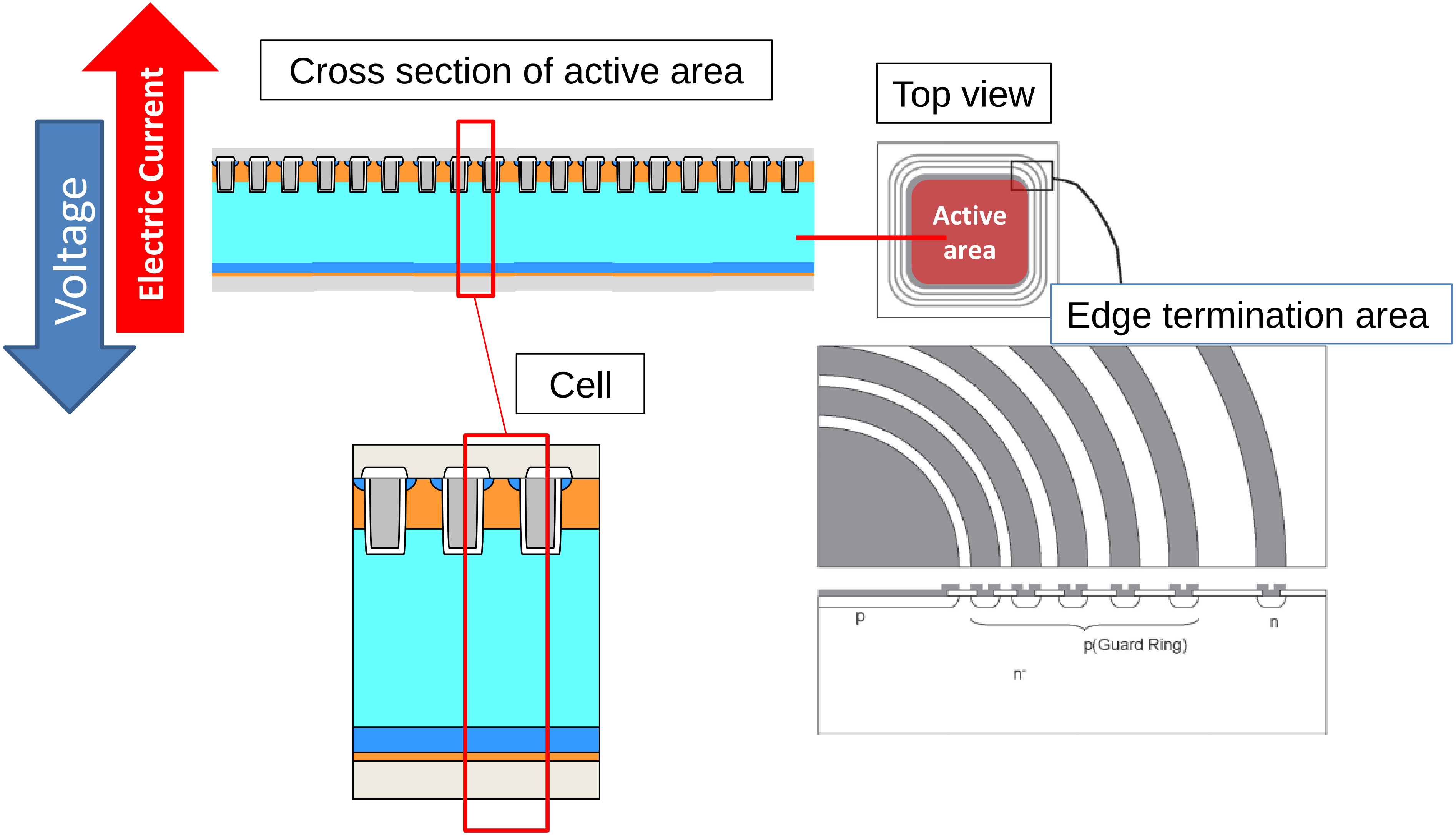


Current control + Bipolar

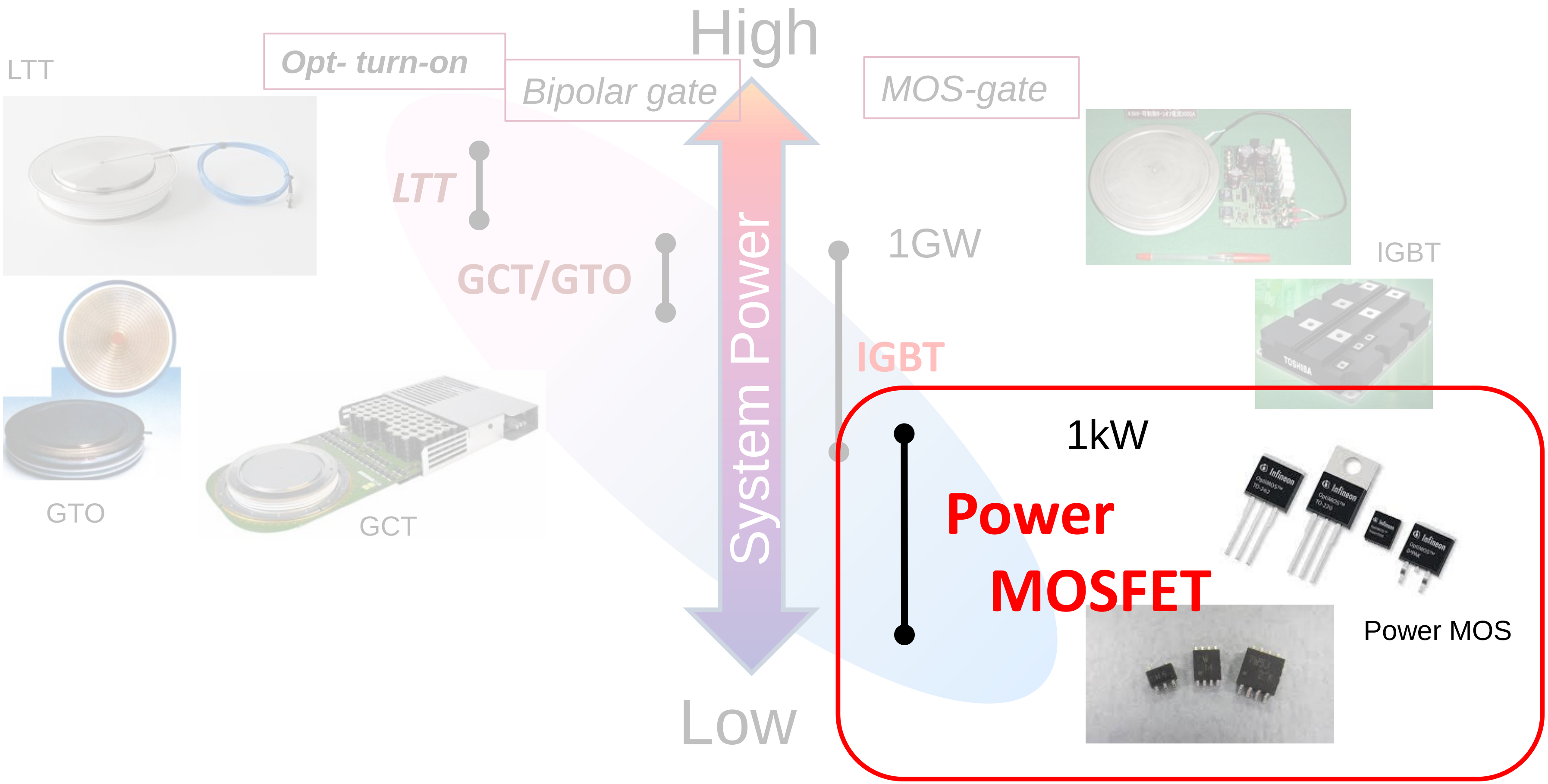
IGBT: Insulated Gate Bipolar Transistor
GTO: Gate Turn-off Thyristor
GCT: Gate Commutated Turn-off Thyristor

1. MOS-gate (voltage) control or bipolar gate (current) control
2. Unipolar conduction or bipolar conduction in high resistive layer(N^-)

Remark: Vertical Device Structure

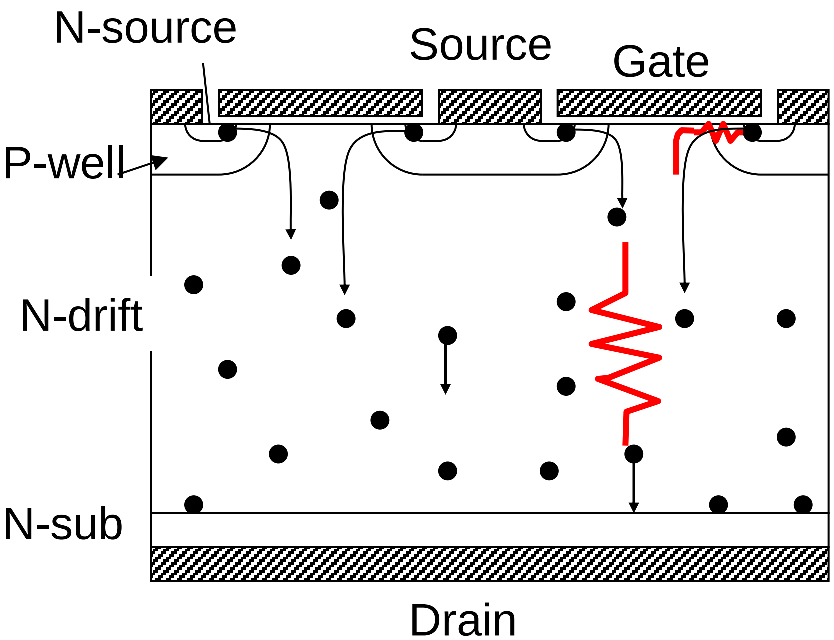


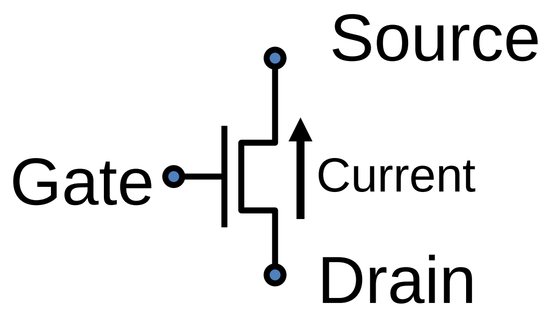
Power MOSFET

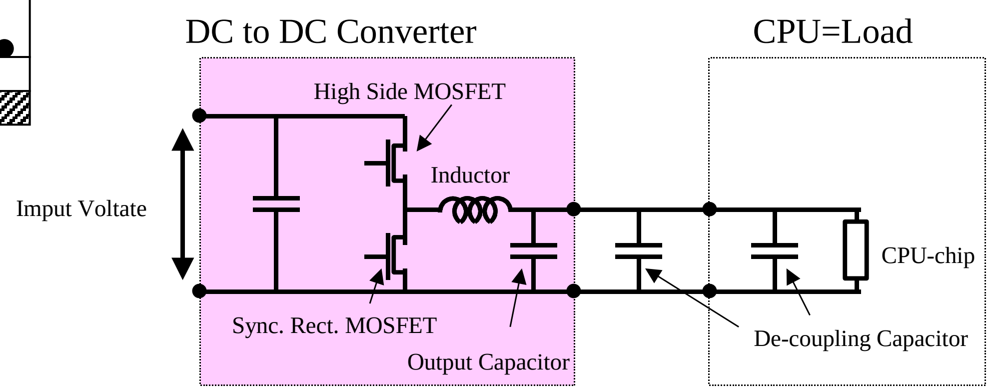


Photos:
Infineon
Toshiba
ABB
TMEIC

Power MOSFET



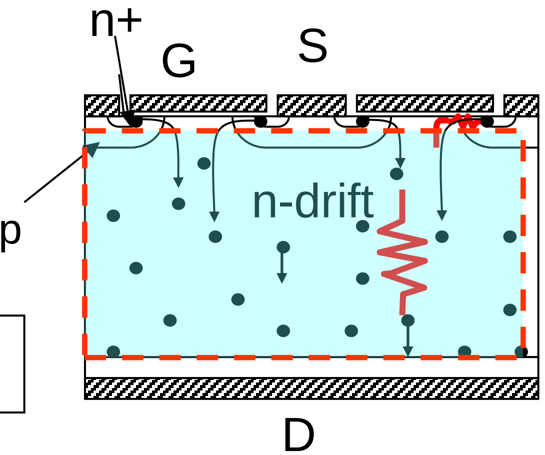




Conduction carrier…… *Electron or hole*
Switching control ……. *MOS-gate*
Switching Freq. ………. *High*

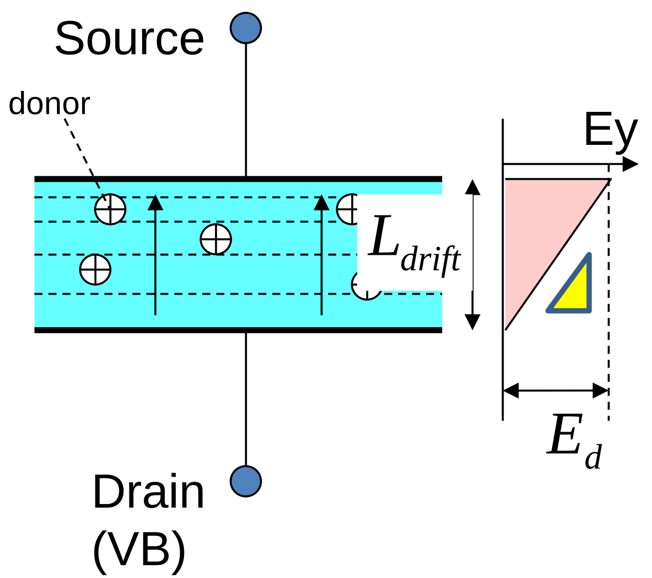
Function of N-drift layer

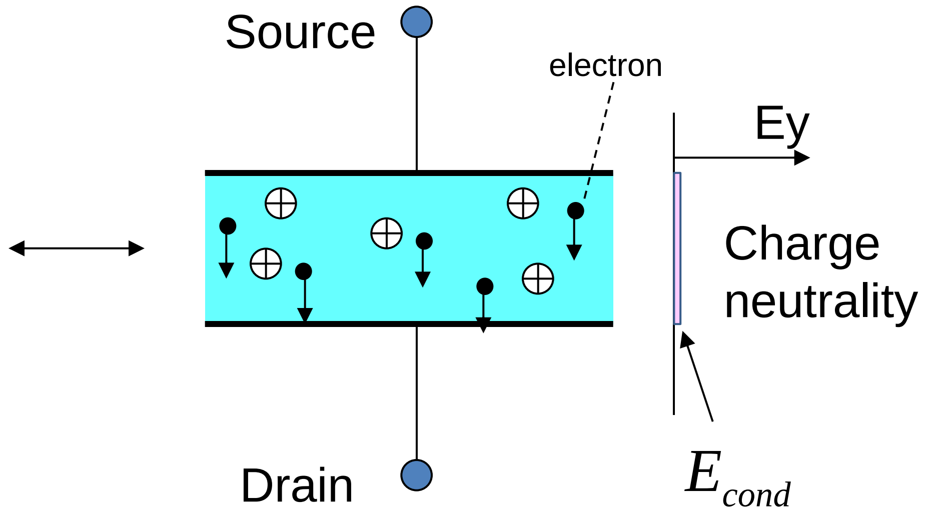
Function of N-drift layer:
1. **Voltage blocking (higher breakdown voltage)**
2. **Current conduction (lower resistivity)**



Voltage Blocking

Conduction





Blocking state (Poisson eq.)

$$qN_D = -\varepsilon \frac{dE_y}{dy} = \varepsilon \cdot \frac{E_d}{L_{drift}}$$

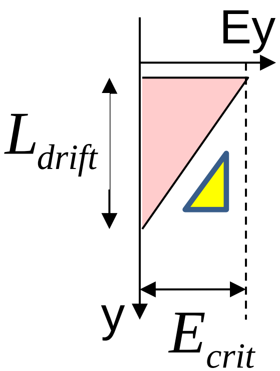
Conduction state (current eq.)

$$J_n = q\mu_n N_D E_{cond} = q\mu_n N_D \frac{V_{cond}}{L_{drift}}$$

μ_n: electron mobility

Drift layer doping, length and drift layer resistance

Ichiro Omura Kyushu Inst. Tech.



$$\begin{cases} V_B = \dfrac{1}{2} E_{crit} \times L_{drift} \\ qN_D = \varepsilon \cdot \dfrac{E_{crit}}{L_{drift}} \end{cases}$$

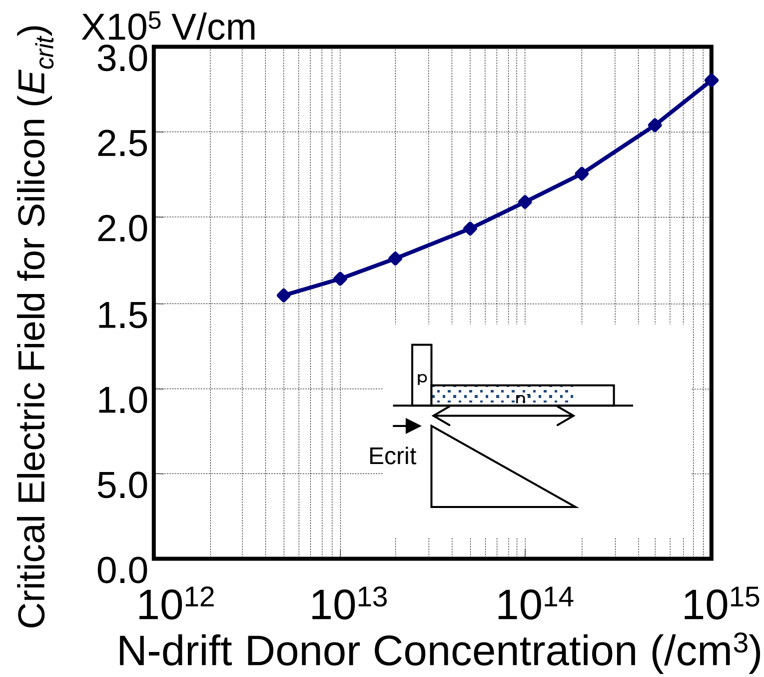
E_{crit}: critical E-field strength

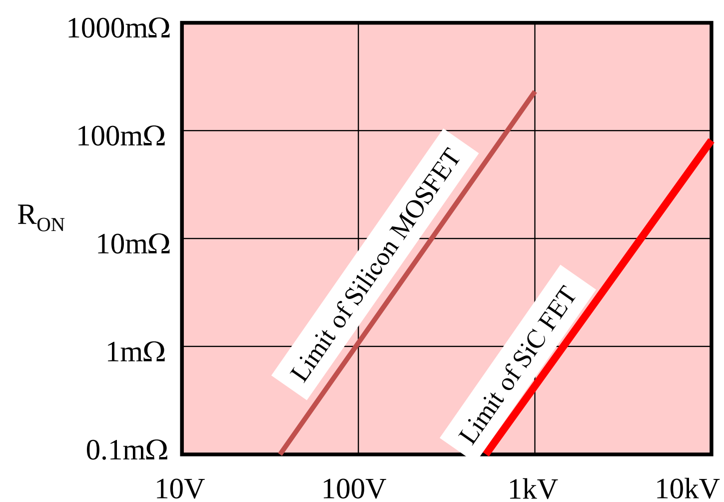
Drift layer doping $$N_D = \varepsilon \cdot \frac{E_{crit}^{2}}{2qV_B}$$

Drift layer length $$L_{drift} = \frac{2V_B}{E_{crit}}$$

$$J_n = q\mu_n N_D \frac{V_{cond}}{L_{drift}}$$

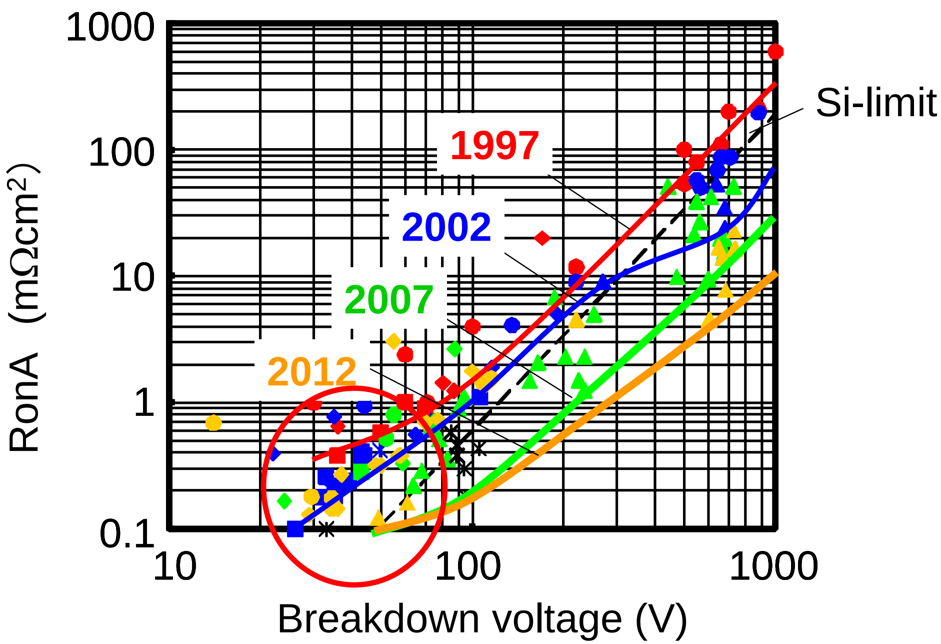
Drift layer resistance [Ωcm²] $$R_{drift} = \frac{4V_B^{2}}{\mu_n \varepsilon E_{crit}^{3}}$$

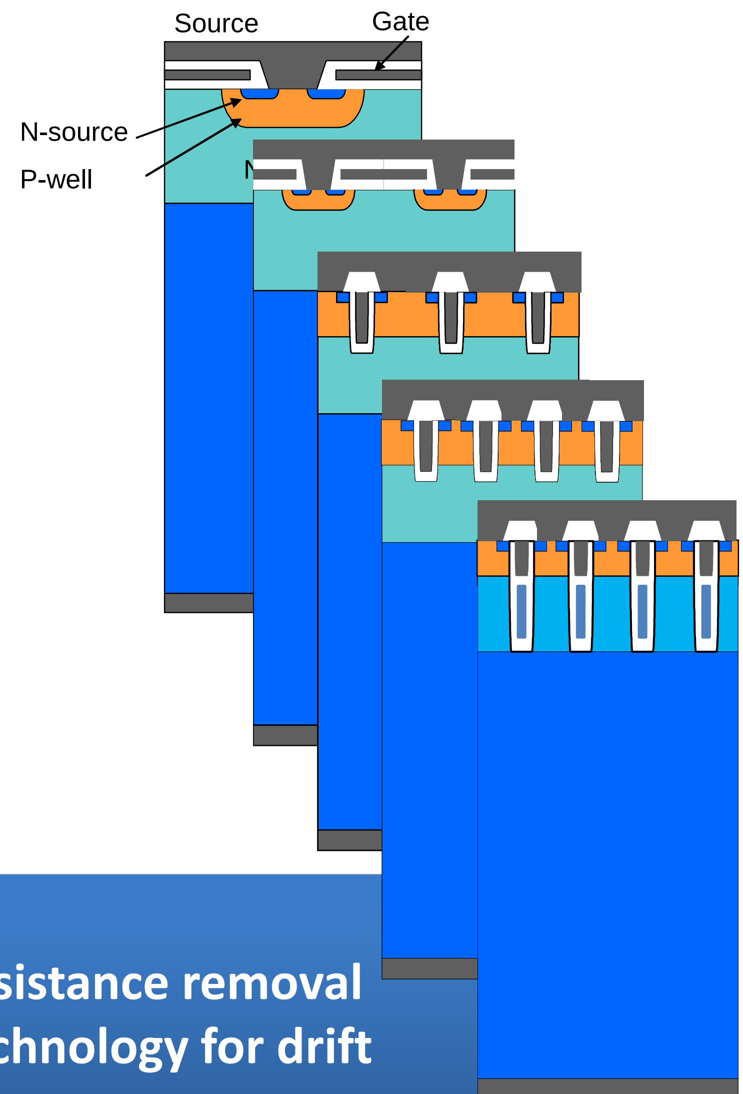




Low Voltage MOSFET (Vertical)

Fig from Lecture Slide by
W. Saito, Toshiba

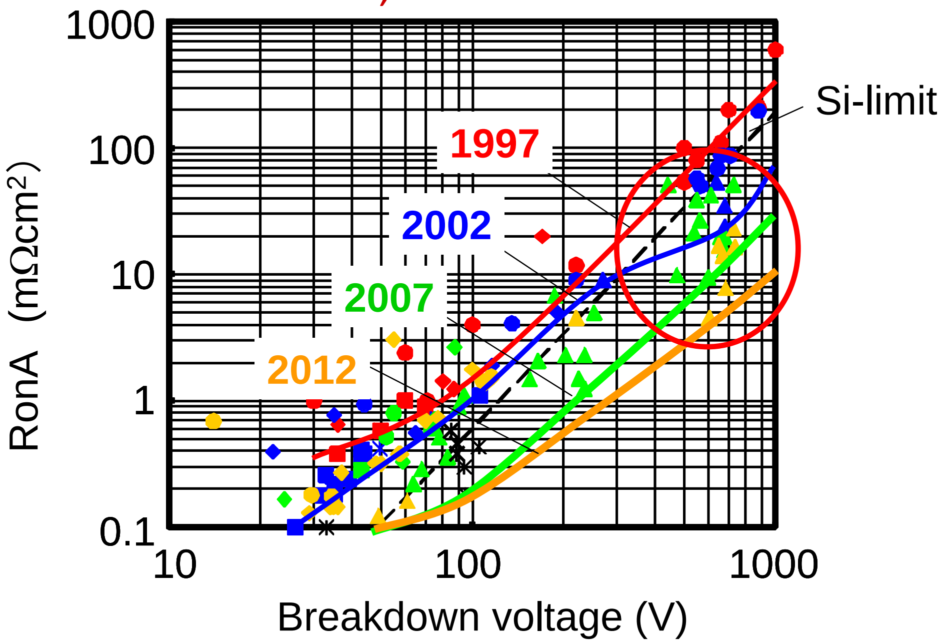


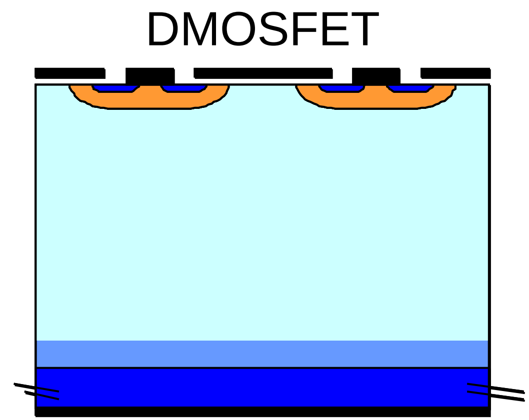


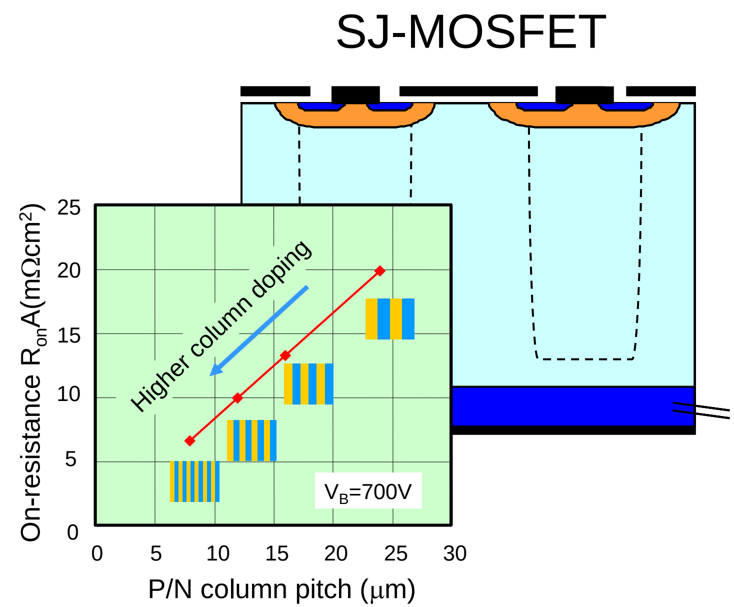
1. **Cell size reduction for channel density**
2. **Trench gate for channel density and JFET resistance removal**
3. **Charge compensate (Vertical Field Plate) technology for drift resistance reduction.**

Super Junction MOSFET

Fig from Lecture Slide by
W. Saito, Toshiba







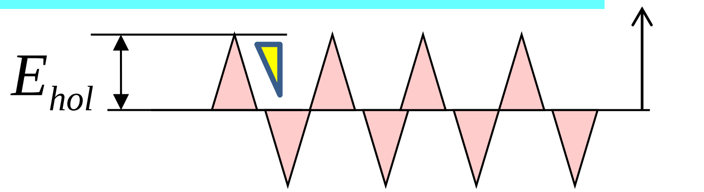
P/N column drift layer
➔Easy to deplete for high impurity concentration
➔Low Ron + High Breakdown Voltage

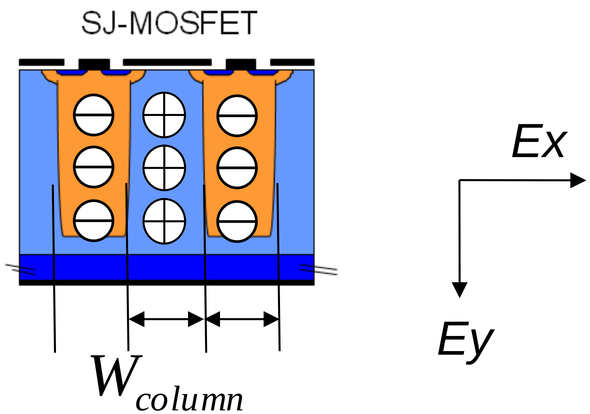
Charge compensate (Super Junction) technology for drift resistance reduction.

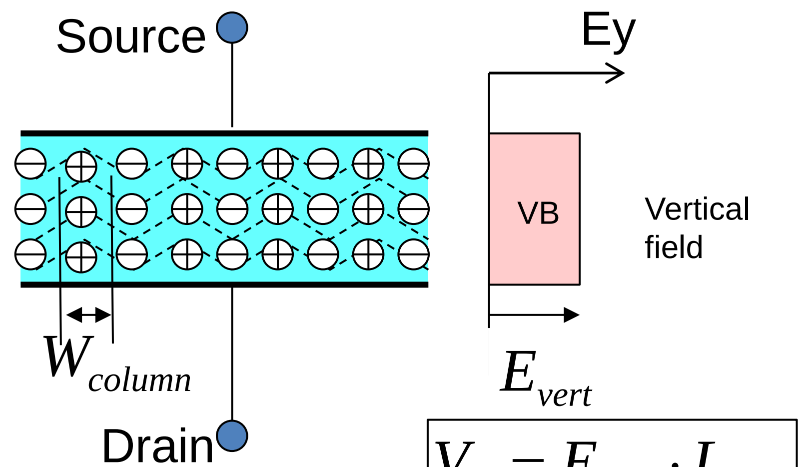
Column doping(N_D) and Breakdown Voltage(V_B)

1. Horizontal field for P/N column depletion

$$qN_D = \varepsilon \frac{dE_x}{dx} = \varepsilon \cdot \frac{2E_{hol}}{W_{column}}$$







$$V_B = E_{vert} \cdot L_{drift}$$

2.Vertical field for voltage blocking between drain and source

3. A half area of drift layer contribute current conduction

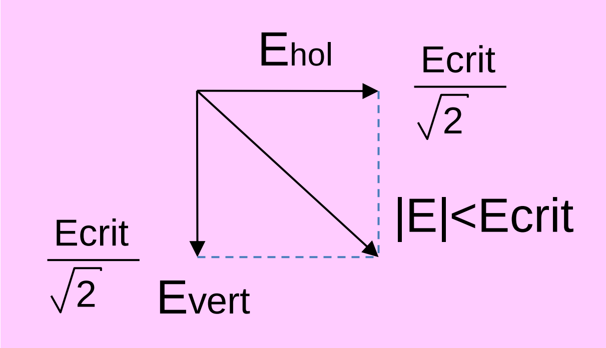
$$J_n = \frac{1}{2} q\mu_n N_D E_{cond}$$

Electric field in SuperJunction structure → high drift layer donor doping

1. **Horizontal electric field for depletion of PN junction in narrow columns**
2. **Vertical electric field for sustain blocking voltage across drift layer**

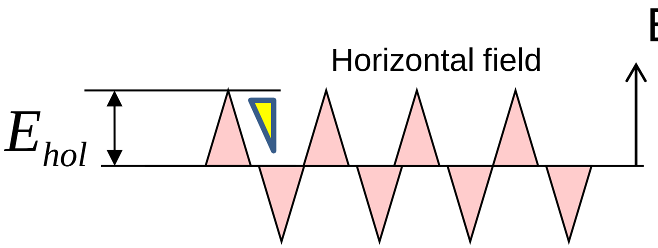
Drift layer doping, length and drift layer resistance

$$\begin{cases} qN_D = \varepsilon \cdot \dfrac{2E_{hol}}{W_{column}} & E_{hol} \Leftarrow \dfrac{E_{crit}}{\sqrt{2}} \\[2ex] V_B = E_{vert} \cdot L_{drift} & E_{vert} \Leftarrow \dfrac{E_{crit}}{\sqrt{2}} \end{cases}$$

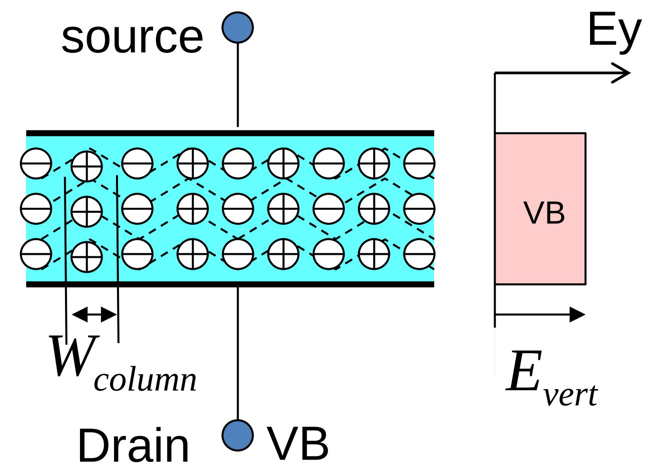


Drift N-column doping $\quad N_D = \varepsilon \cdot \dfrac{\sqrt{2}E_{crit}}{qW_{column}}$

Drift layer length $\quad L_{drif} = \dfrac{\sqrt{2}\,V_B}{E_{crit}}$



$$J_n = \frac{1}{2} q\mu_n N_D E_{cond} = \frac{1}{2} q\mu_n N_D \frac{V_{cond}}{L_{drift}}$$

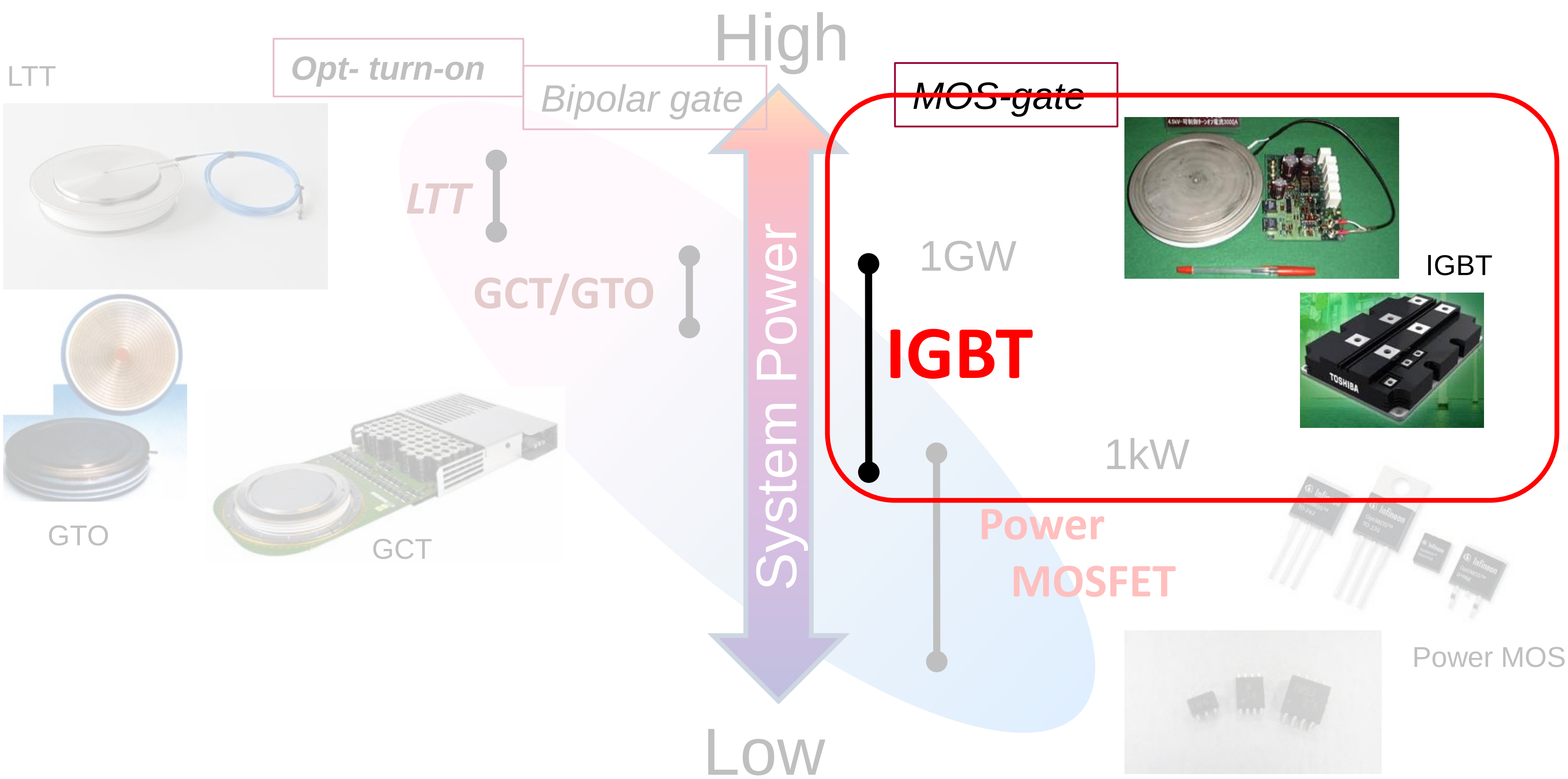


Drift layer resistance [Ωcm²] $\quad R_{drift} = \dfrac{2V_B \cdot W_{colomn}}{\mu_n \varepsilon\, E_{crit}^2}$

Assumption: N-column and P-column are same width

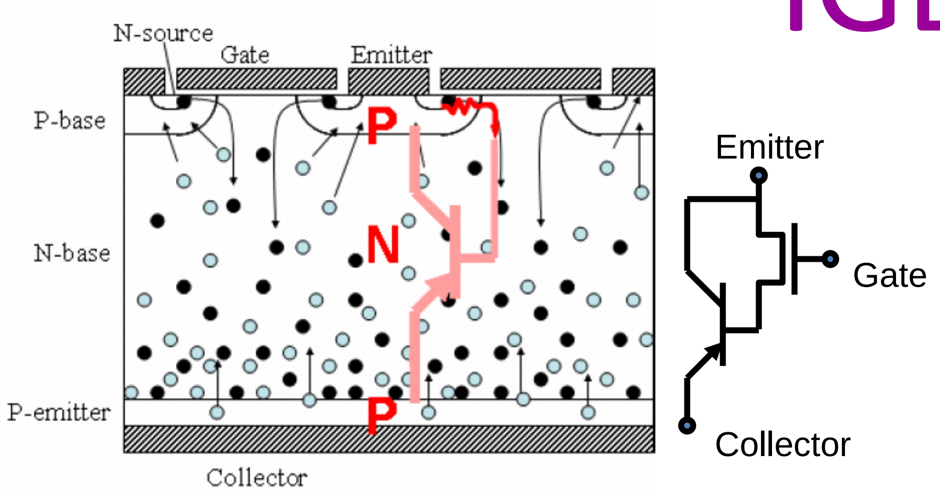
IGBT

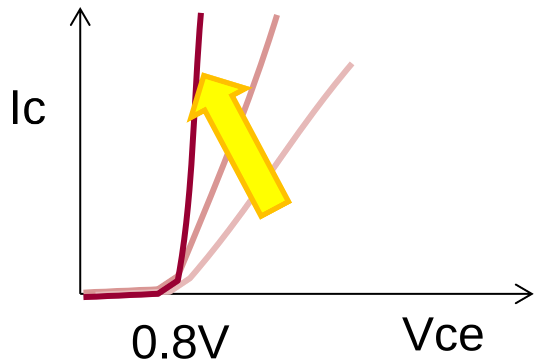
Insulated Gate Bipolar Transistor



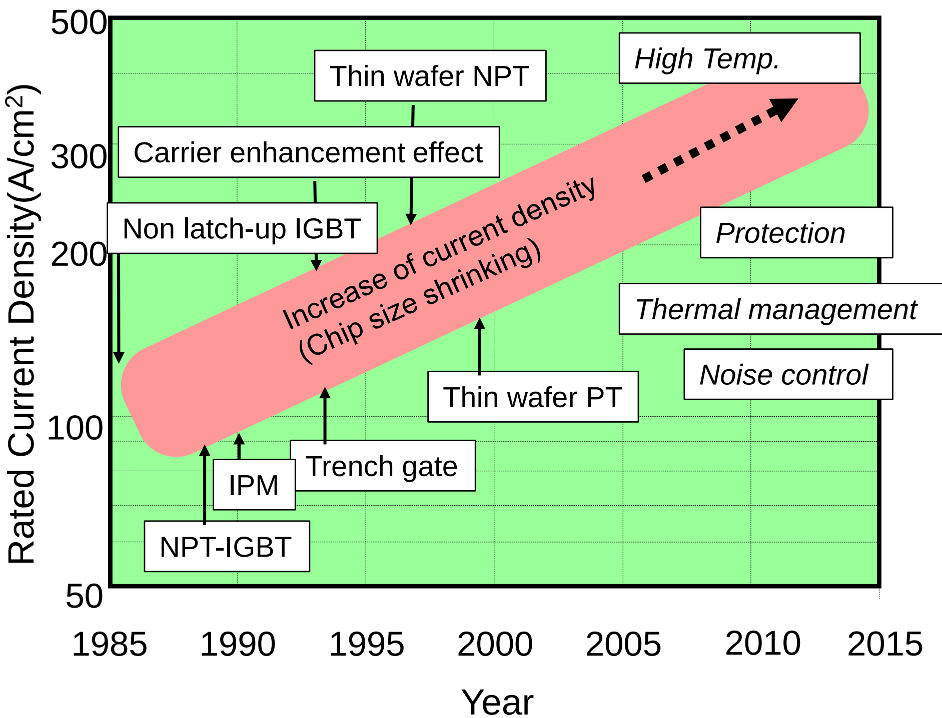
Photos:
Infineon
Toshiba
ABB
TMEIC

IGBT





Shen, Omura, “Power Semiconductor Devices for Hybrid, Electric, and Fuel Cell Vehicles” Proc. Of the IEEE, Issue 4, 2007



1. **Bipolar Transistor + MOSFET (before IE-effect)**
2. **High current capability**
3. **~0.8V collector-emitter threshold voltage for conduction**
4. **Medium switching speed (15kHz for motor drive, 100kHz for ICT current supply and FPD driver)**

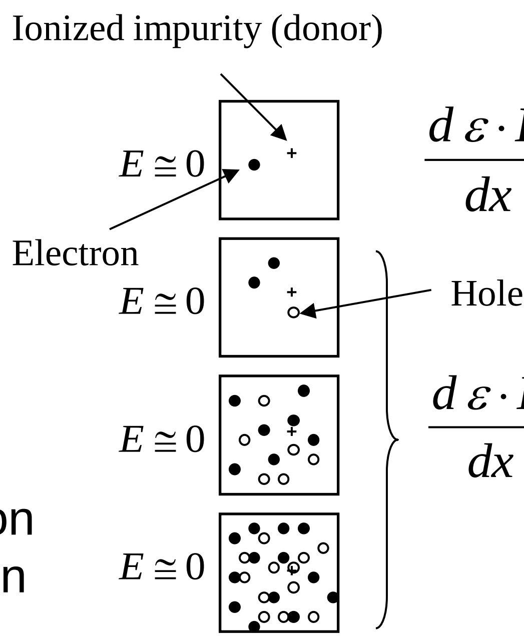
Operation mechanism of IGBT

Conduction modulation in N-base

Unipolar

↓

Conduction modulation



$$\frac{d\,\varepsilon\cdot E}{dx} = q(\overset{\text{positive}}{N_D} - \overset{\text{negative}}{n}) \cong 0$$

$$\frac{d\,\varepsilon\cdot E}{dx} = q(N_D + p - n) \cong 0$$

$$N_D << p,n \longrightarrow n_i << p \cong n$$

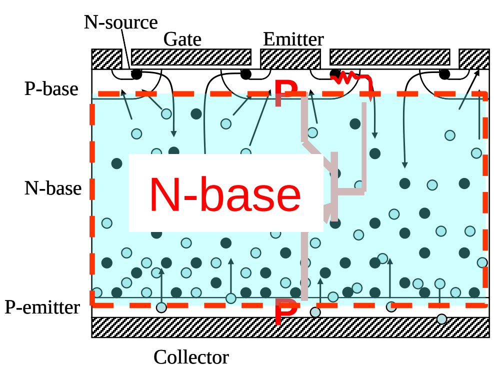
$$pn = n_i^2$$

$$\phi_p \cong \phi_n$$

↓

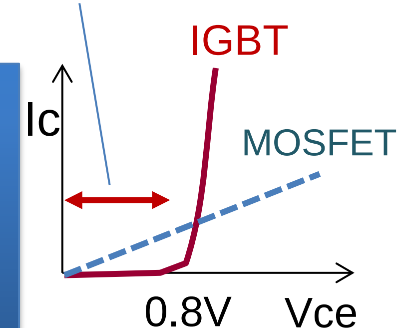
$$\boxed{pn = n_i^2 e^{\frac{q}{kT}(\phi_p - \phi_n)}}$$

PN-junction built-in potential

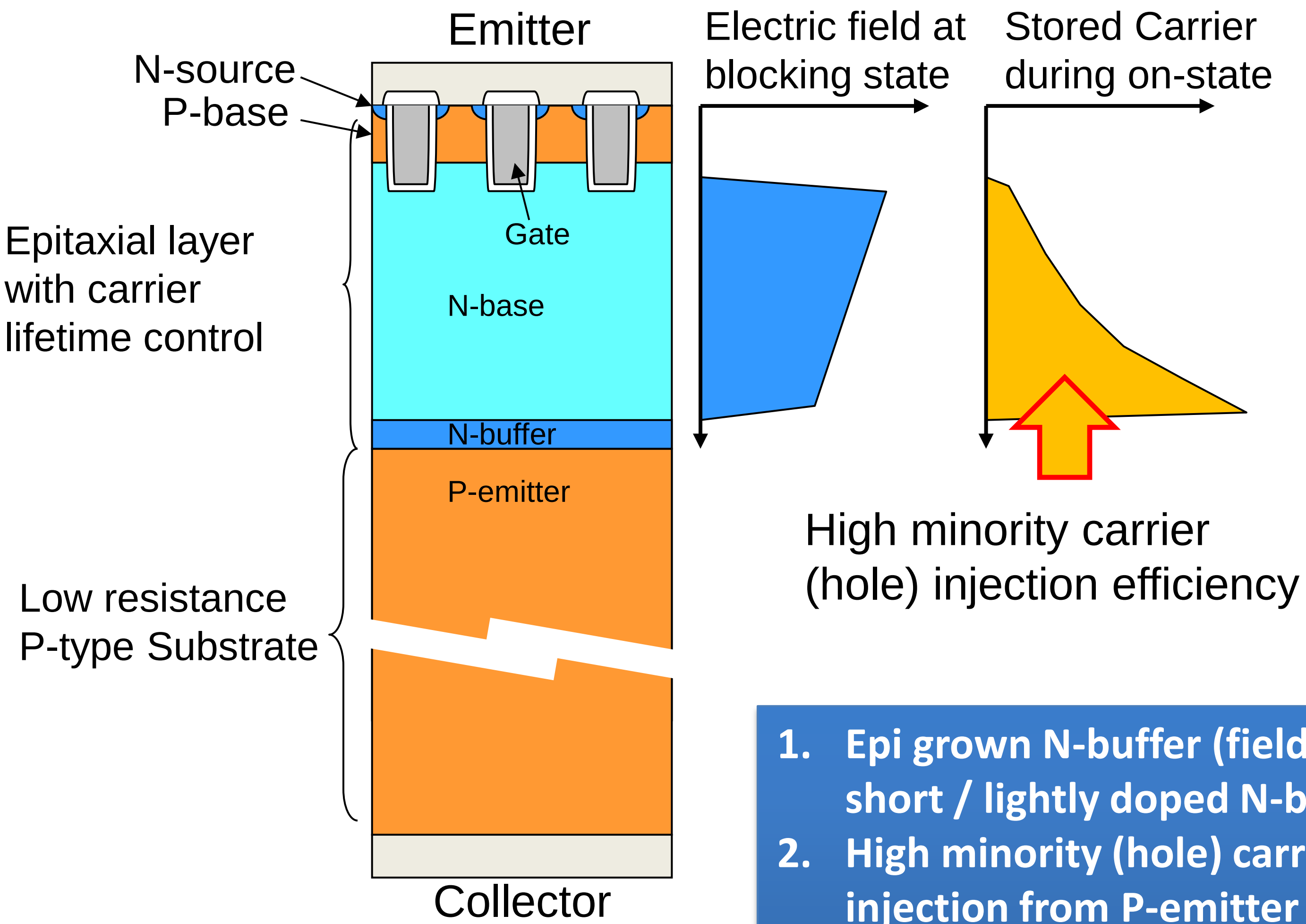


Conduction modulation

1. **Both hole and electron contribute to current conduction**
2. **High stored carrier density in N-base (>10^{16}cm^{-3})**
3. **Built-in voltage with the stored carrier**

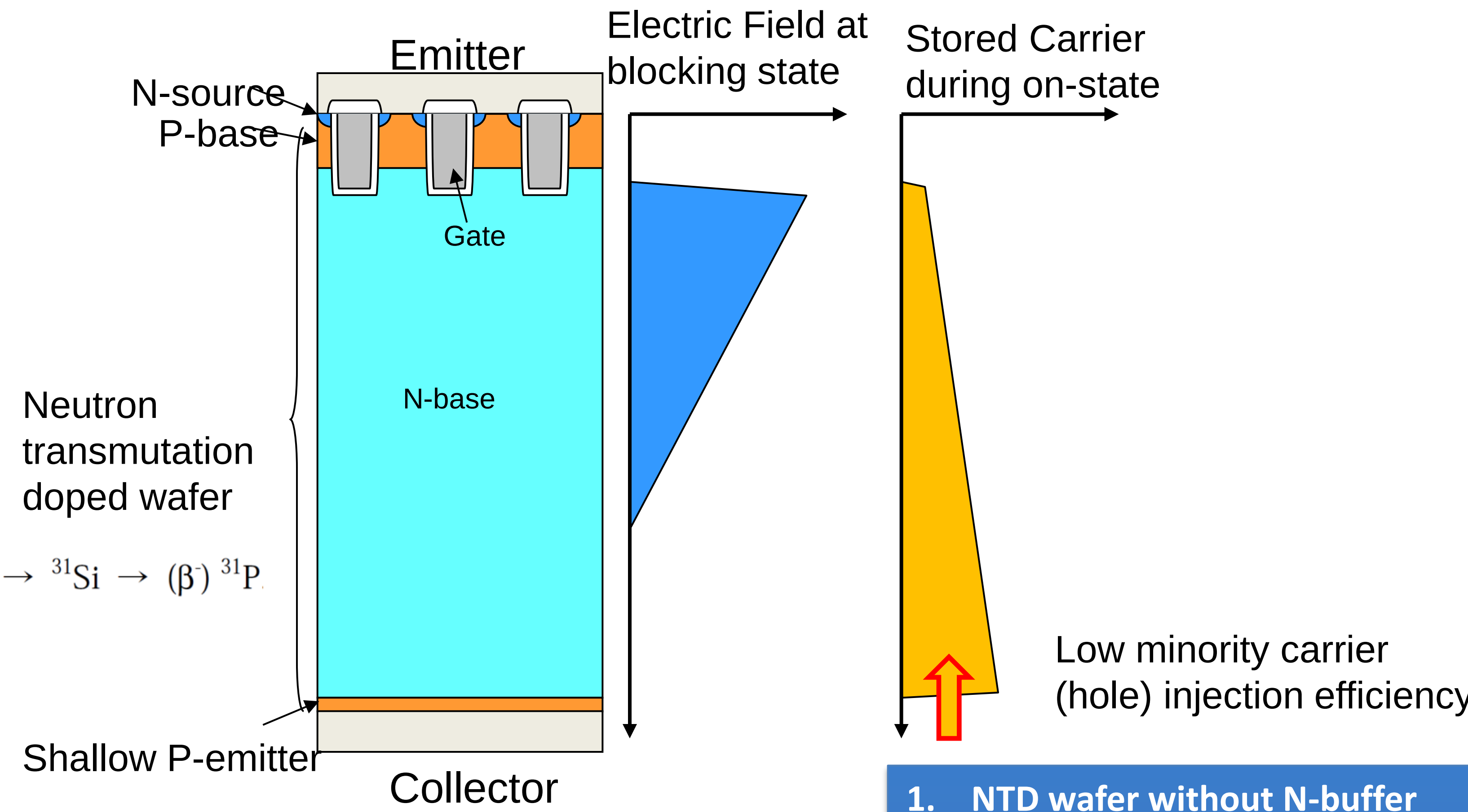


Punch-through IGBT (PT-IGBT)



1. **Epi grown N-buffer (field stop) and short / lightly doped N-base**
2. **High minority (hole) carrier injection from P-emitter**
3. **Low-conduction loss and large switching loss**
4. **Carrier lifetime control (high energy electron irradiation etc.) required**

Non-Punch-through IGBT (NPT-IGBT)



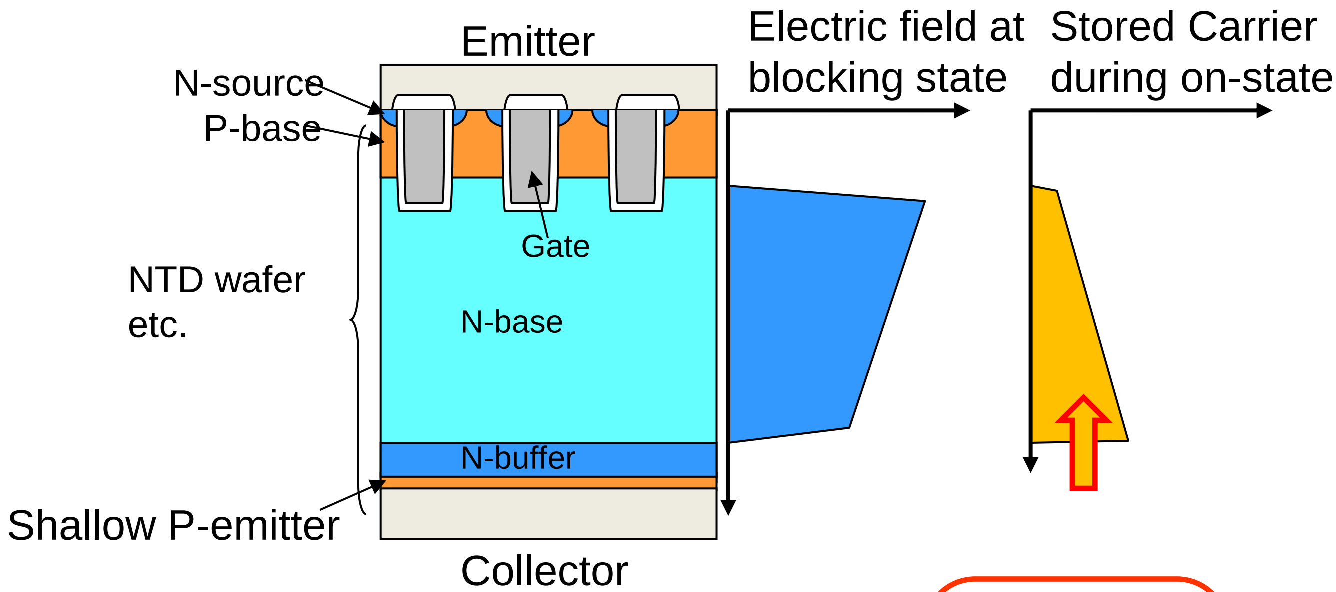
$^{30}\mathrm{Si} + \mathrm{n} \rightarrow {}^{31}\mathrm{Si} \rightarrow (\beta^-)\ {}^{31}\mathrm{P}$

1. **NTD wafer without N-buffer**
2. **Low minority (hole) carrier injection from P-emitter**
3. **Higher-conduction loss and lower switching loss**
4. **No carrier lifetime control required**

Neutron transmutation doping

M. Tanenbaum and A. D. Mills J. Electrochem. Soc., vol. 108, pp.171 1961
J. Cornu and R. Sittig IEEE Trans. Electron Devices, vol. ED-22, pp.108 1975
IAEA-TECDOC-1681, Neutron Transmutation Doping of Silicon at Research Reactors, 2012

Thin wafer IGBT technology



	PT	NPT	Thin-wafer-PT
N-base length	Short	Long	Short
P-emitter hole injection	High	Low	Low
Carrier lifetime in N-base	Short	Long	Long

=FS-IGBT

Thin Wafer Technology

-Reduction of turn-off tail current with short N-base

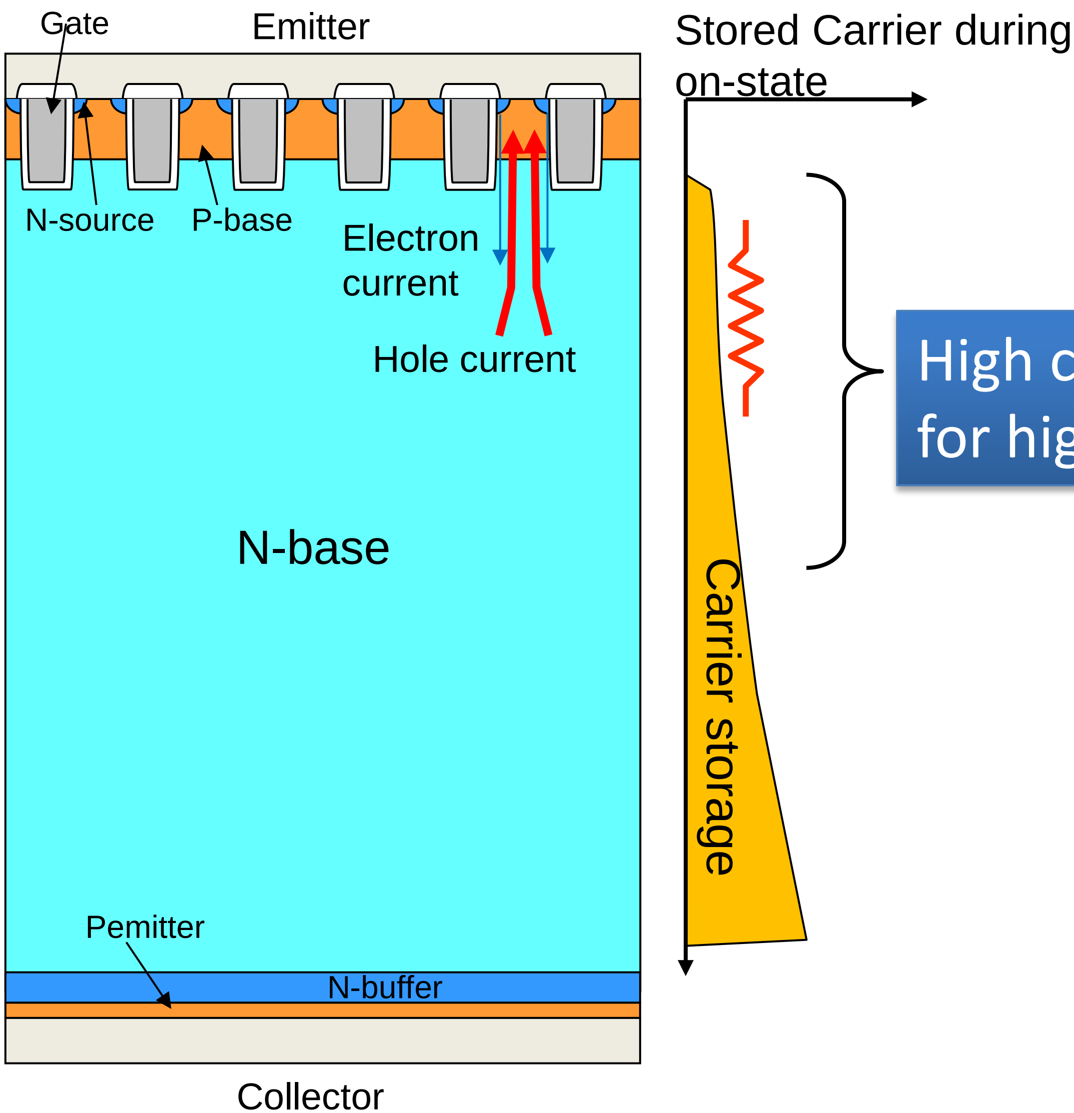
-Reduction of conduction loss with short N-base

Low Hole Injection P-emitter with long carrier lifetime

-Reduction of turn-off tail current with low hole injection

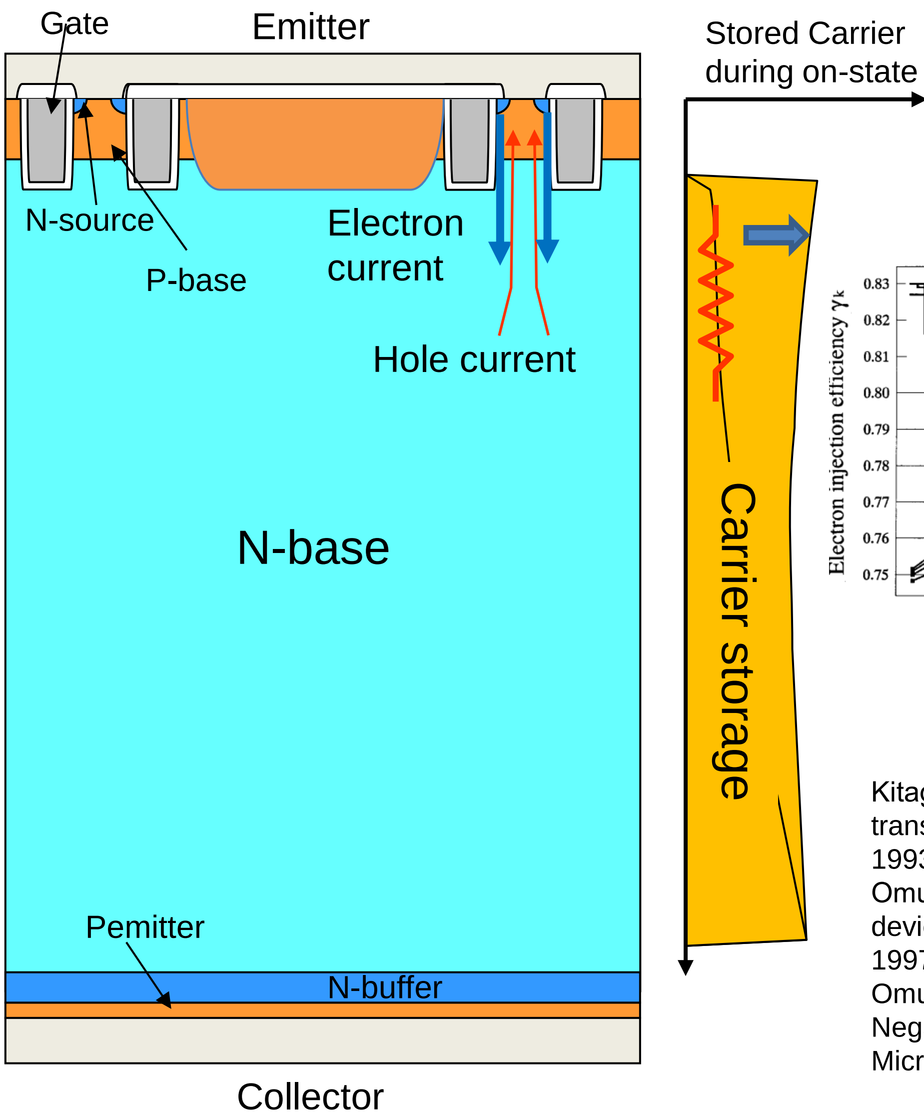
-Better thermal coefficient without carrier lifetime control

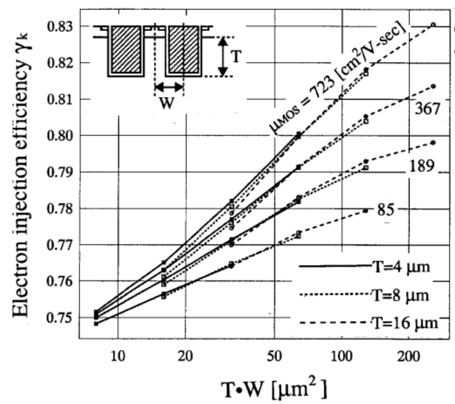
Problem in High Voltage IGBT Device Design

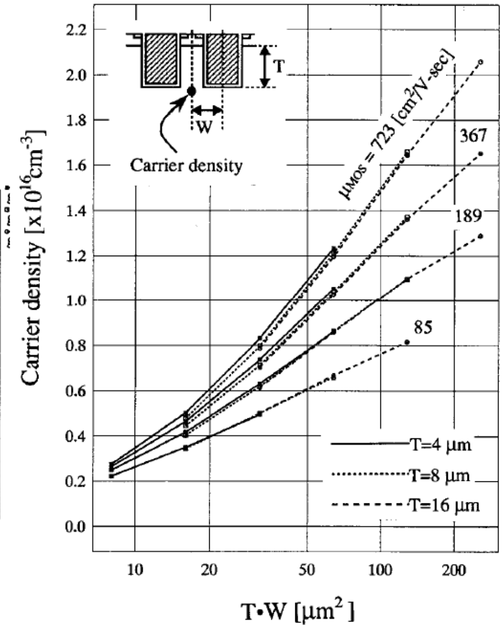


High conduction resistance for high voltage IGBT

Electron Injection Enhancement Effect





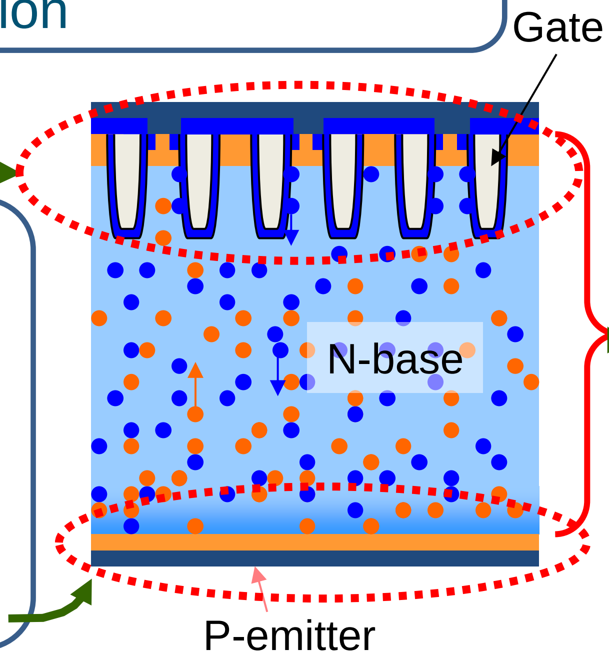


Kitagawa et al. "A 4500 V injection enhanced insulated gate bipolar transistor (IEGT) operating in a mode similar to a thyristor," IEDM'93, 1993.
Omura et al. "Carrier injection enhancement effect of high voltage MOS devices-device physics and design concept," ISPSD 97, pp. 217-220, 1997.
Omura, "High Voltage MOS Device Design: Injection Enhancement and Negative Gate Capacitance, (ETH thesis 2000), Series in Microelectronics Vol. 150, Hartung-Gorre Verlag, 2005.

Trench gate technology with special structure enhances majority carrier (electron) injection in N-base ➔ Low conduction loss under high current density

Summary of IGBT Technology

- Trench Gate
  - Conduction loss reduction with electron injection enhancement
  - Channel resistance, JFET resistance reduction

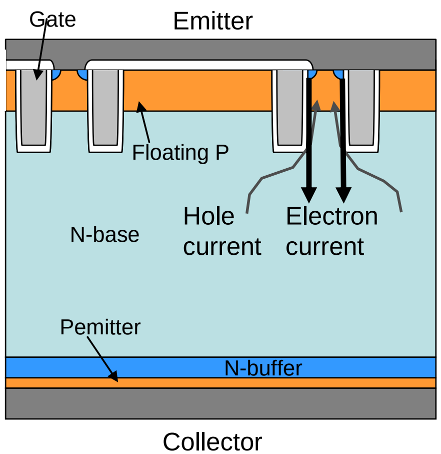


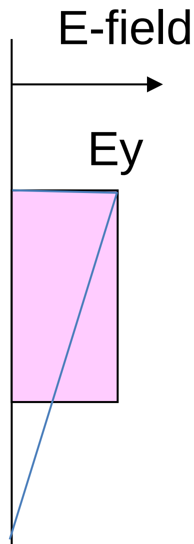
- Low Injection P-emitter + Long Carrier Lifetime
  - Turn-off loss reduction with low hole storage in N-base
  - Better thermal coefficient without carrier lifetime control

- Thin Wafer Technology
  - Both conduction and turn-off loss reduction with with short N-base

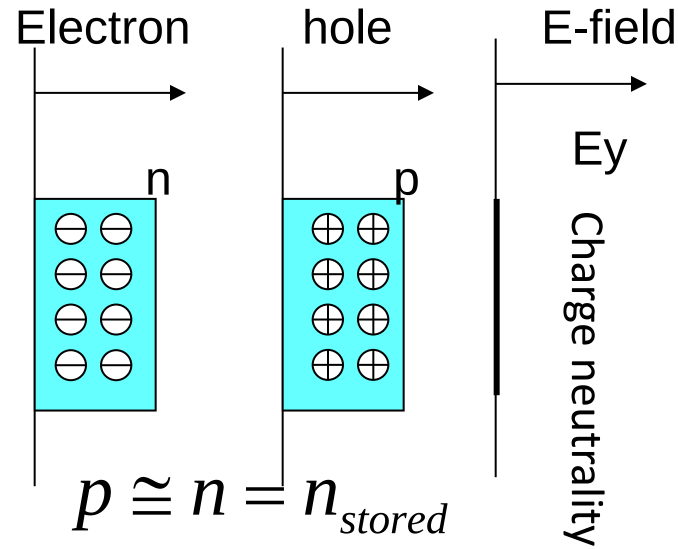
Conduction and Breakdown Voltage

Voltage blocking





Conduction
(flat carrier distribution is assumed)



$$p \cong n = n_{stored}$$

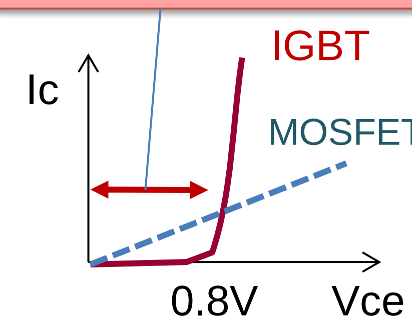
N-base length $$2\frac{V_B}{E_{crit}} \geq L_{n-base} \geq \frac{V_B}{E_{crit}}$$

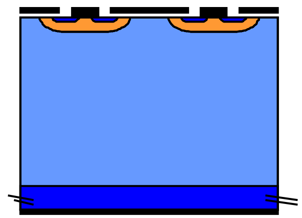
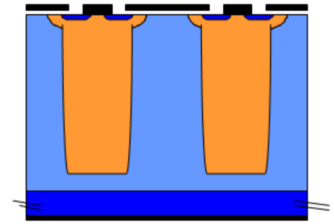
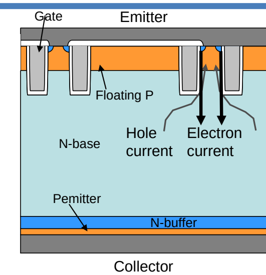
Stored Carrier density $$n_{stored}$$

PN-junction built-in potential

$$V_{built-in} = 2\frac{kT}{q}\ln\frac{n_{stroed}}{n_i}$$

N-base conduction resistance $$R_{N-base} = \frac{1 \sim 2\,V_B}{q(\mu_n + \mu_p)\cdot n_{stored}\cdot E_{crit}}$$

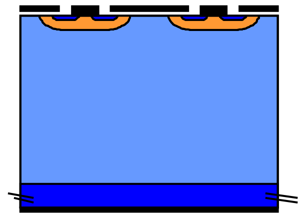
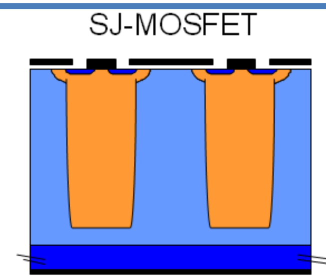
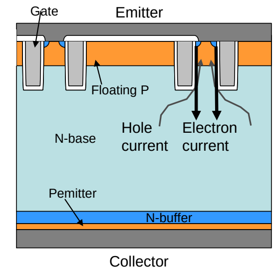
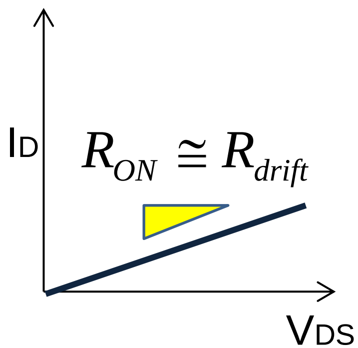
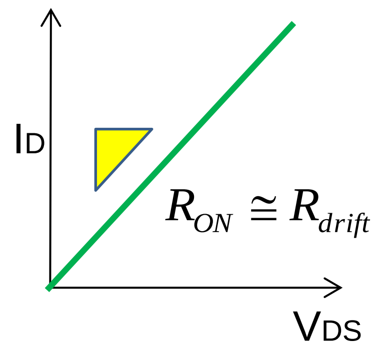
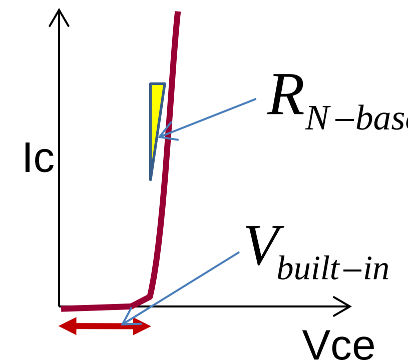
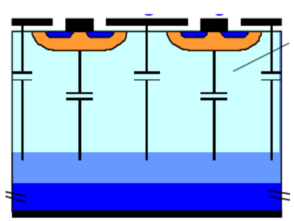
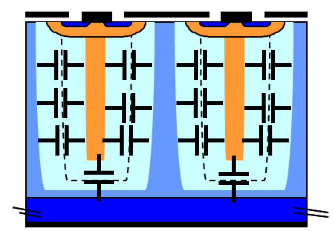
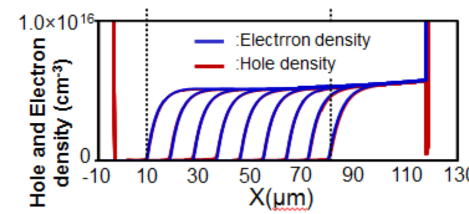


	DMOSFET	SJ-MOSFET	IGBT
Device Structure			
Drift Layer Doping (Stored carrier density)	$N_D = \varepsilon \cdot \frac{E_{crit}^2}{2qV_B}$	$N_D = \varepsilon \cdot \frac{\sqrt{2}E_{crit}}{qW_{column}}$	n_{stored} (>10^{16}cm^{-3})
Drift Layer Length (N-base length)	$L_{drif} = \frac{2V_B}{E_{crit}}$	$L_{drif} = \frac{\sqrt{2}\,V_B}{E_{crit}}$	$L_{n-base} = \frac{1 \sim 2V_B}{E_{crit}}$
Drift Layer Resistance (N-base conduction resistance)	$R_{drift} = \frac{4V_B^2}{\mu_n \varepsilon\, E_{crit}^3}$	$R_{drift} = \frac{2V_B \cdot W_{colomn}}{\mu_n \varepsilon\, E_{crit}^2}$	$R_{N-base} = \frac{1 \sim 2\,V_B}{q(\mu_n + \mu_p) \cdot n_{stored} \cdot E_{crit}}$
PN-junction built-in potential	none	none	$V_{built-in} = 2\frac{kT}{q}\ln\frac{n_{stored}}{n_i}$
600V class device	80-100 mΩcm^2	<10 mΩcm^2	~1.5V at 200A/cm2

Assumption: N-column and P-column are same width

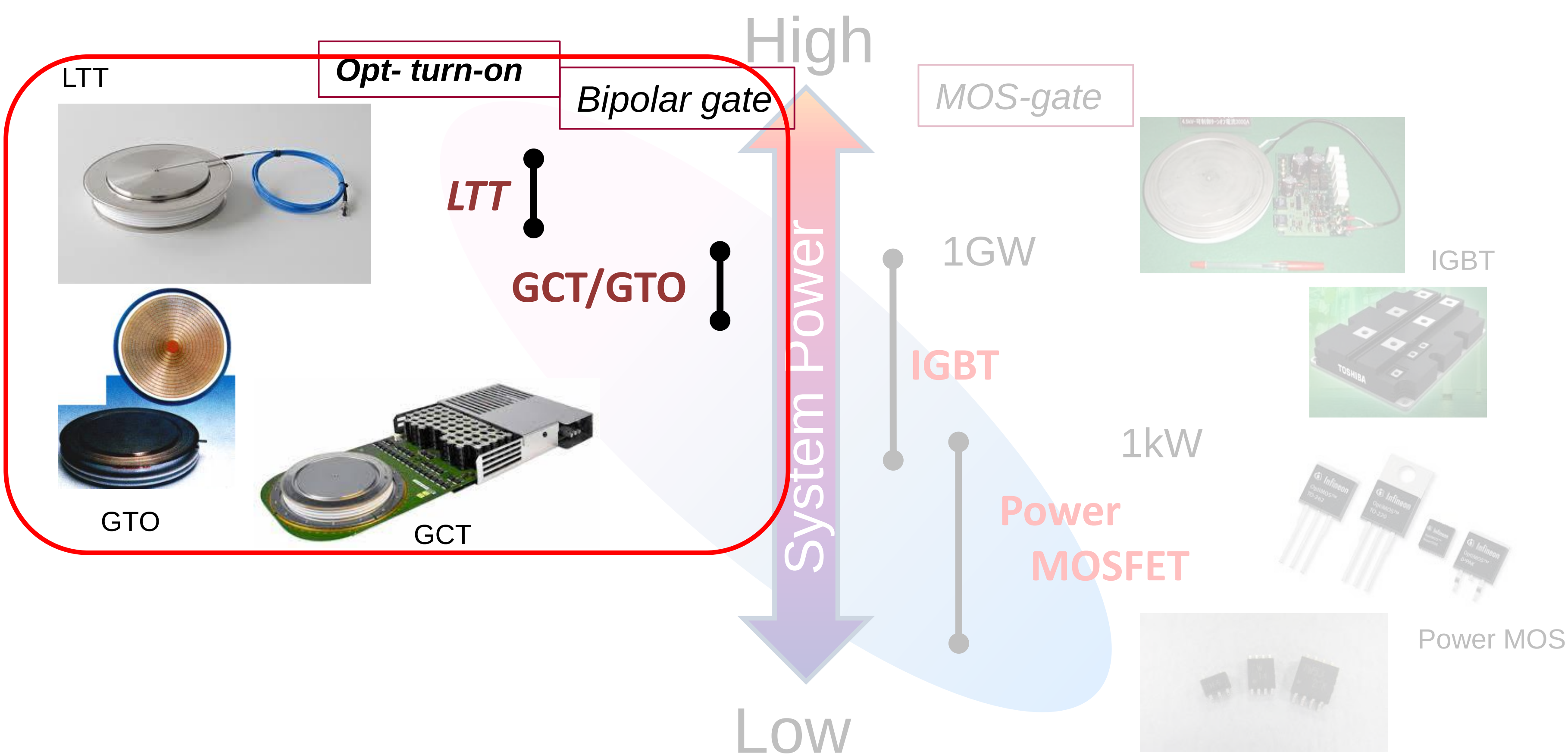
(flat carrier stored carrier distribution is assumed

Omura et. al, International Workshop on Physics of Semiconductor Devices, 2007. IWPSD 2007, pp. 781 – 786, 2007

	DMOSFET	SJ-MOSFET	IGBT
Device Structure			
V-I characteristics			
Switching charge (turn-off charge)	 Charge in main-junction capacitance	 PN-column depletion charge	 Stored carrier sweep out

Omura et. al, International Workshop on Physics of Semiconductor Devices, 2007. IWPSD 2007, pp. 781 – 786, 2007

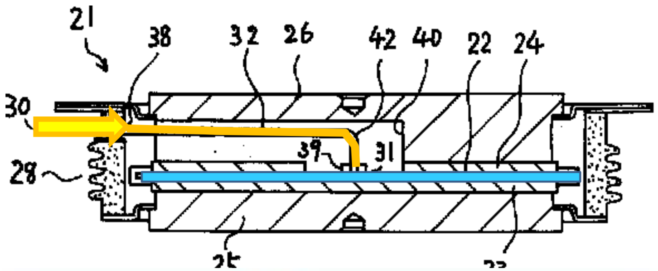
Types of Power Semiconductors

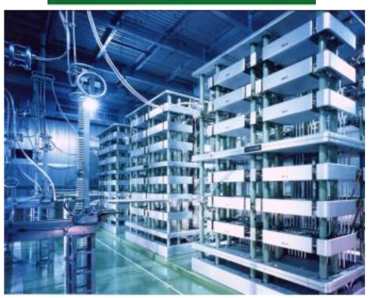


Photos:
Infineon
Toshiba
ABB
TMEIC

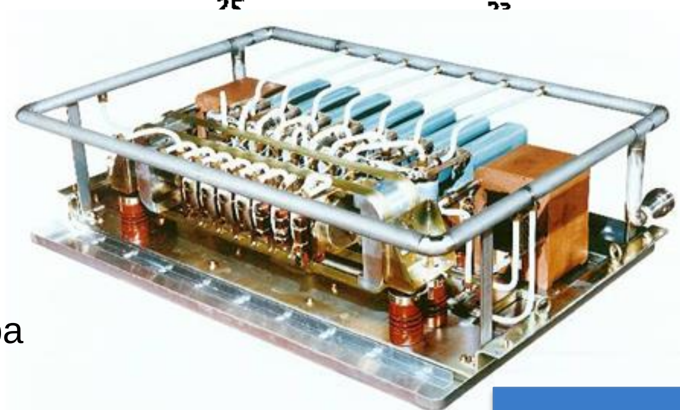
Light Triggered Thyristor(LTT)

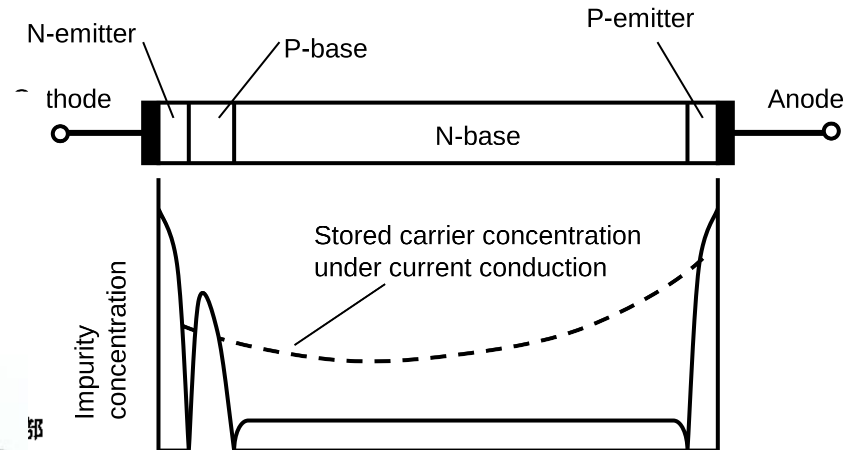
Photos: http://dbnst.nii.ac.jp/

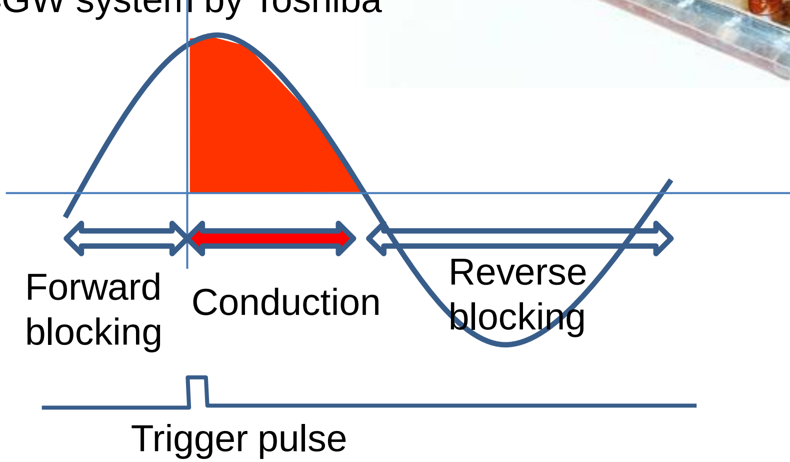




1.4GW system by Toshiba

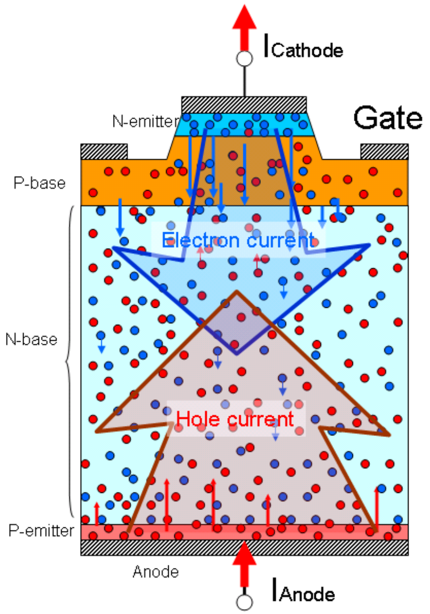


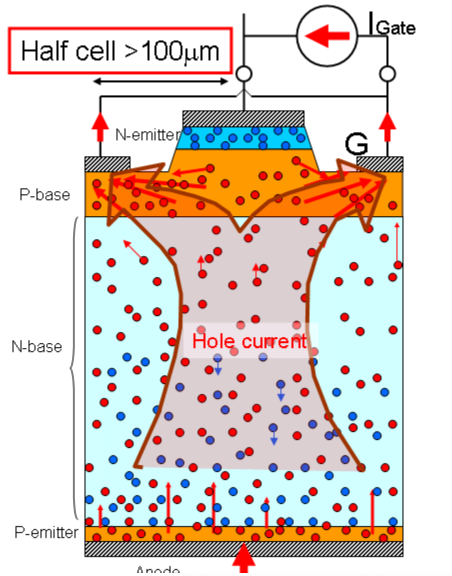




1. **PNPN structure**
2. **Light triggered turn-on**
3. **Cannot turn-off by gate**
4. **One wafer per one device**
5. **Pressure contact package**
6. **Highest power per single semiconductor**

GCT: Gate Commutated Turn-off Thyristor





1. **PNPN structure**
2. **One wafer per one device**
3. **> 100um cell size**
4. **Pressure contact package**
5. **Very low stray inductance integrated gate driver for couple of kA gate current**
6. **Highest power per single semiconductor *turn-off* device**

ABB

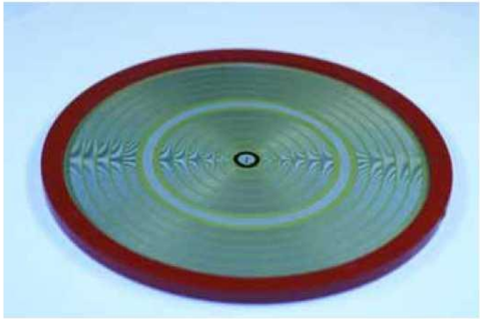
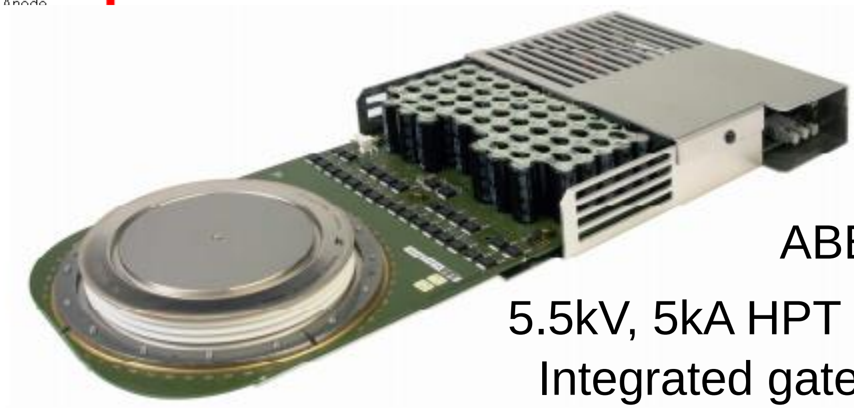


Figure 1: A 91 mm HPT IGCT wafer with approximately 2700 cathode segments organized into ten segment rings. The gate metallization covers the rest of the wafer and surrounds all segments. The gate-contact ring separates the five peripheral segment rings from the central rings.



ABB

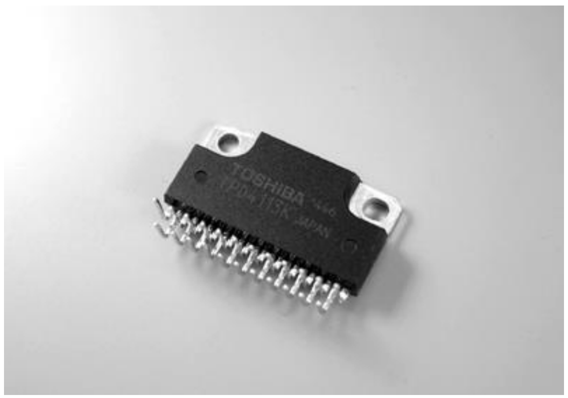
5.5kV, 5kA HPT IGCT
Integrated gate circuit

Lateral Devices

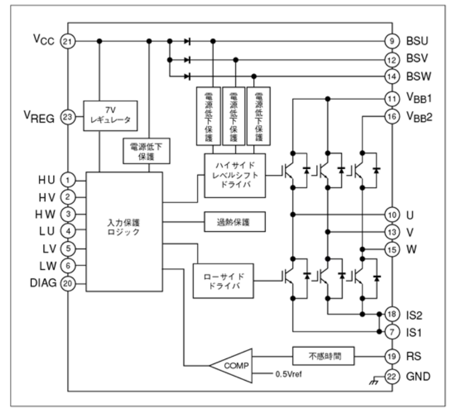
Control and Power = Power IC

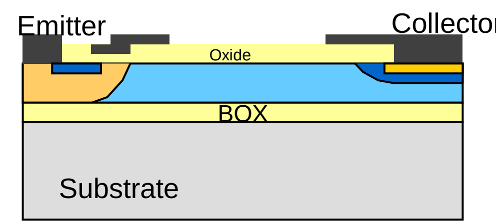
~1kV

Motor Driver



Toshiba

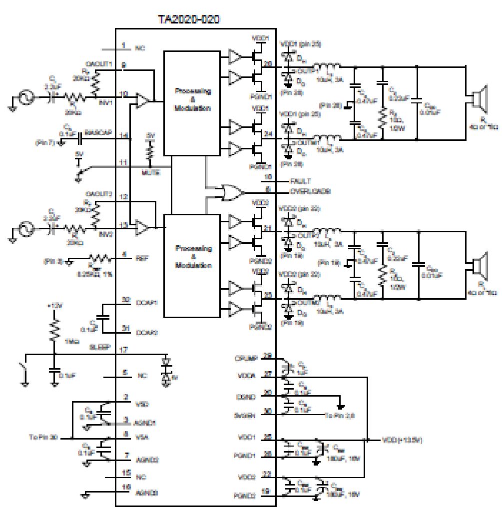


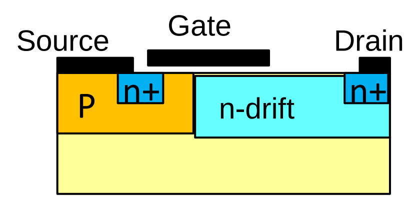


<100V

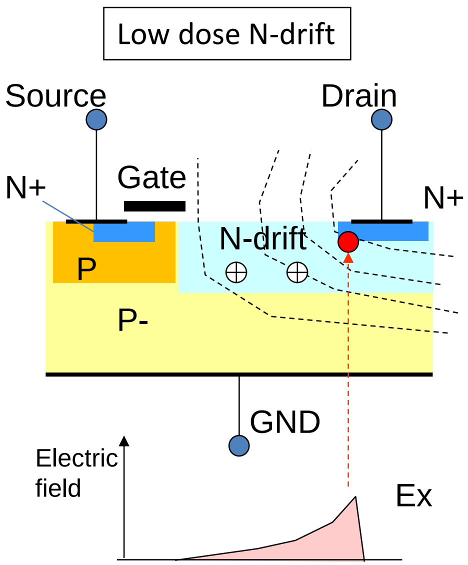
Audio Speaker Driver

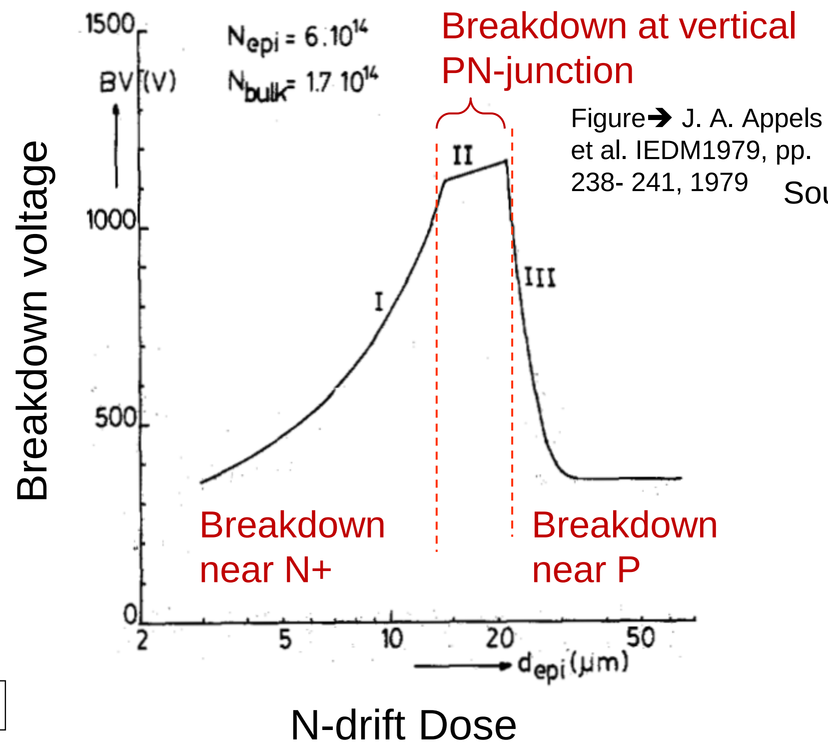
Trypath datasheet

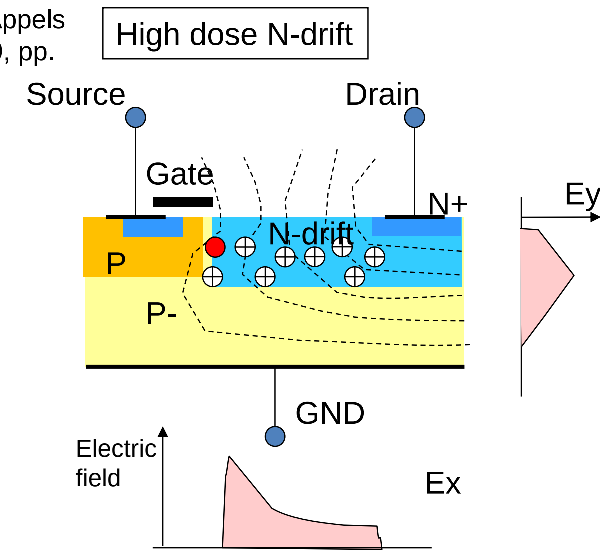


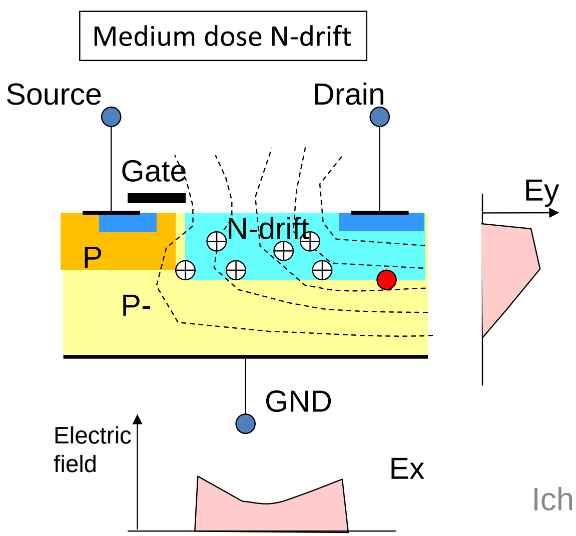


RESURF principle for breakdown voltage design



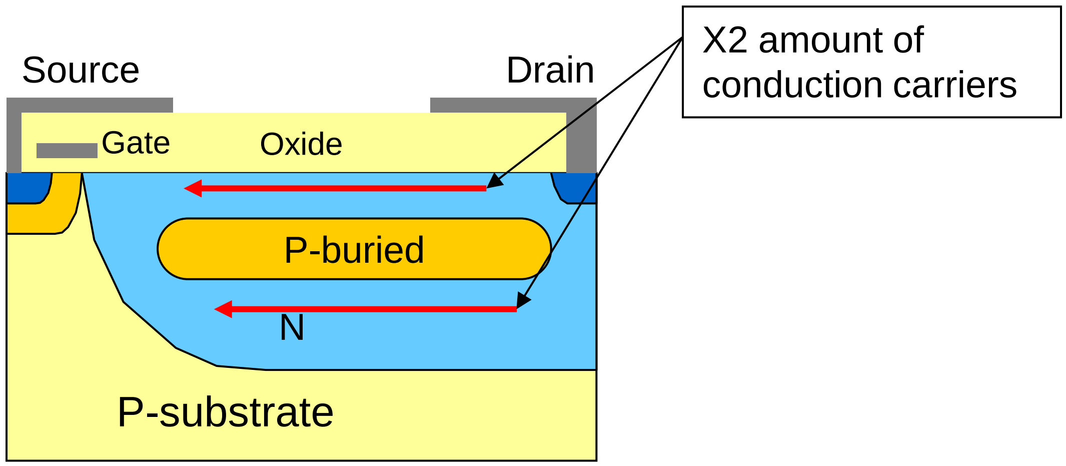


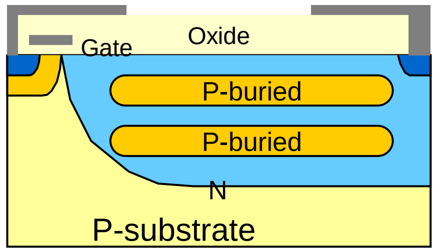




N-drift dose (atm/cm^2) is the key parameter for breakdown voltage design (~1e12/cm2)

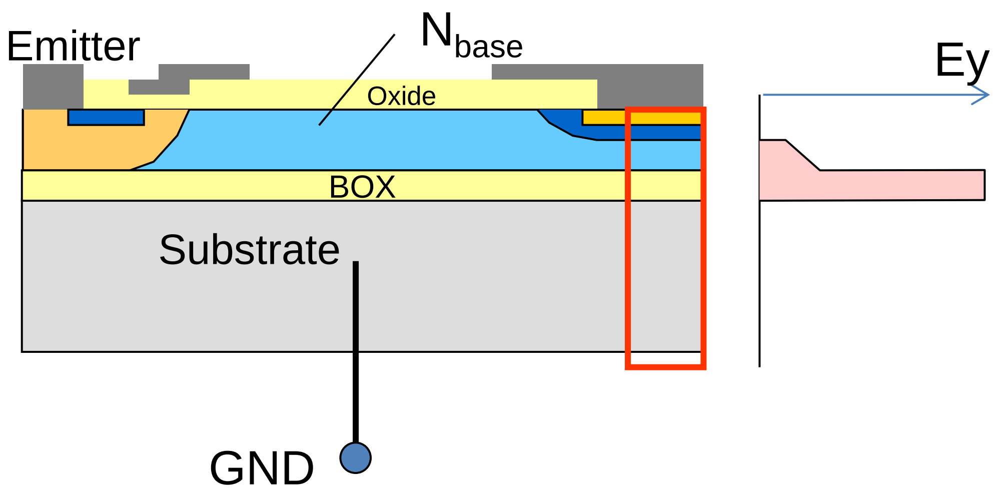
Lateral “Super Junction” MOSFET

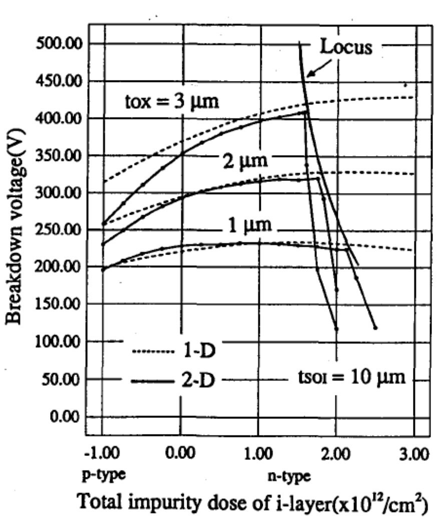




D. Disney et al. A new 600V lateral PMOS device with a buried conduction layer, pp.41-44, ISPSD’ 03

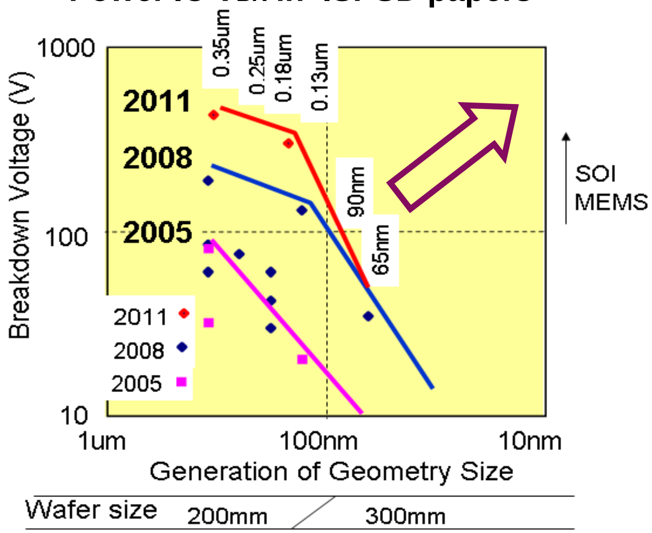
SOI IGBT

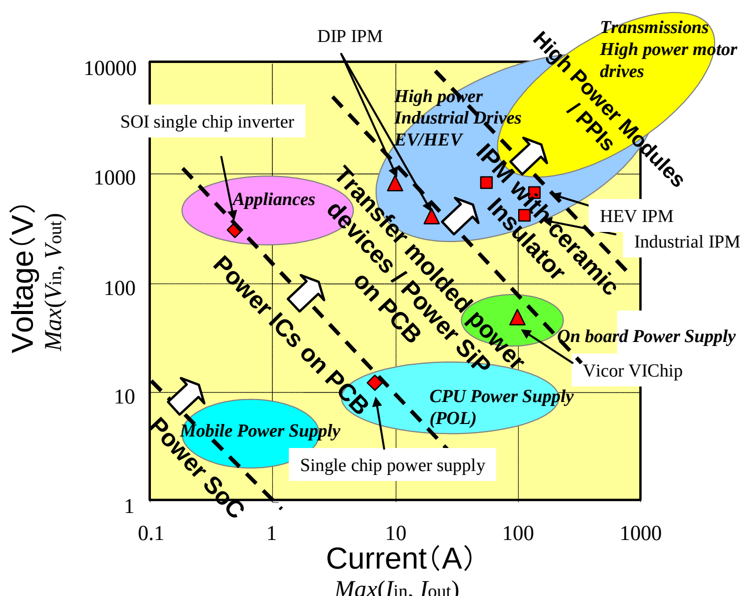




Future Power ICs

Power IC VBK in ISPSD papers





Future HV Power IC will be …

Digital Rich

Power IC

Kilowatt

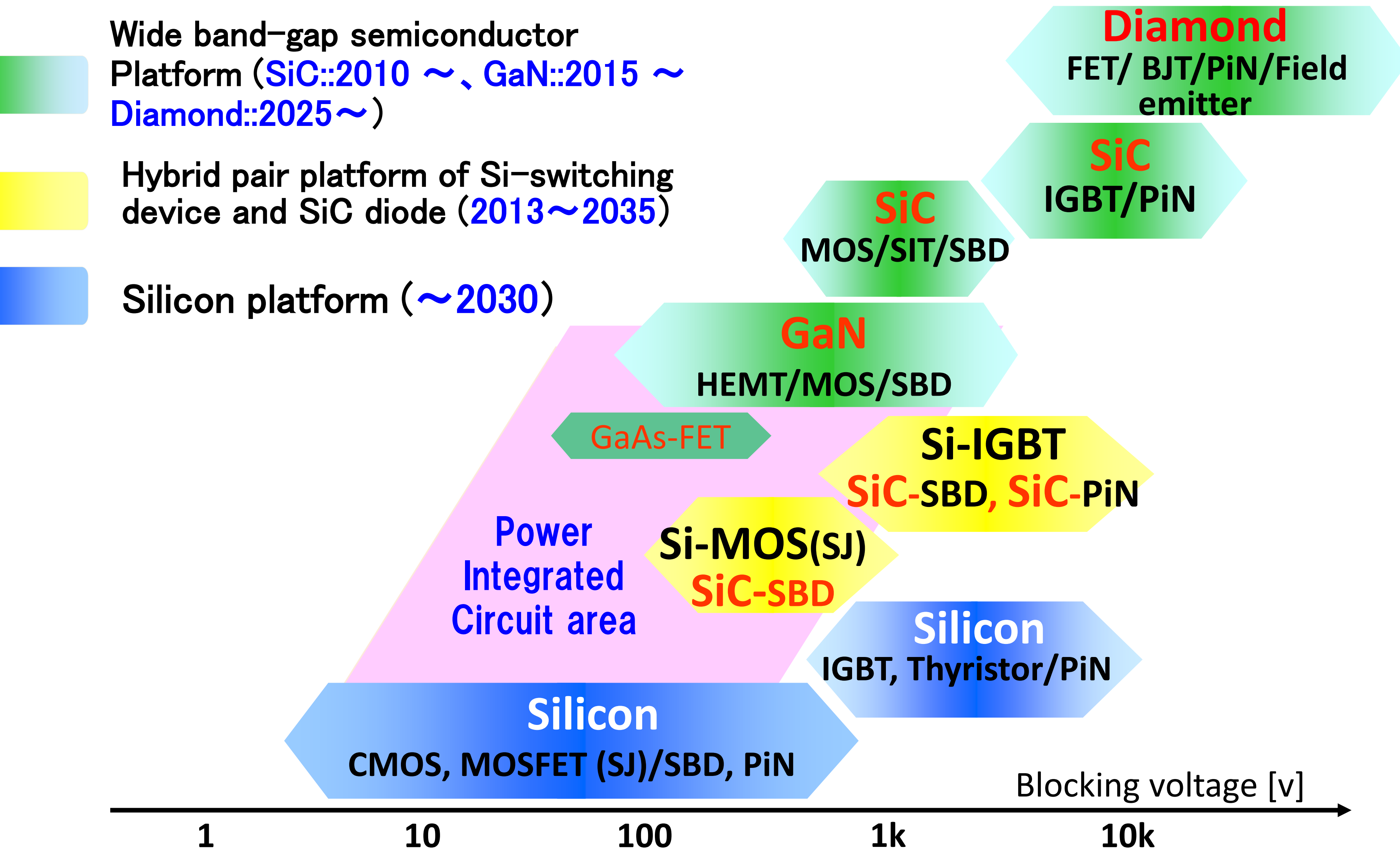
Power IC

Omura, ECPE workshop Jan. 2012

Omura, CIPS 2010

Future Possibility

Advanced power devices Road map



H. Ohashi et al. “Role of Simulation Technology for the Progress in Power Devices and Their Applications,” IEEE T-ED, Vol. 60, issue 2, 2013.

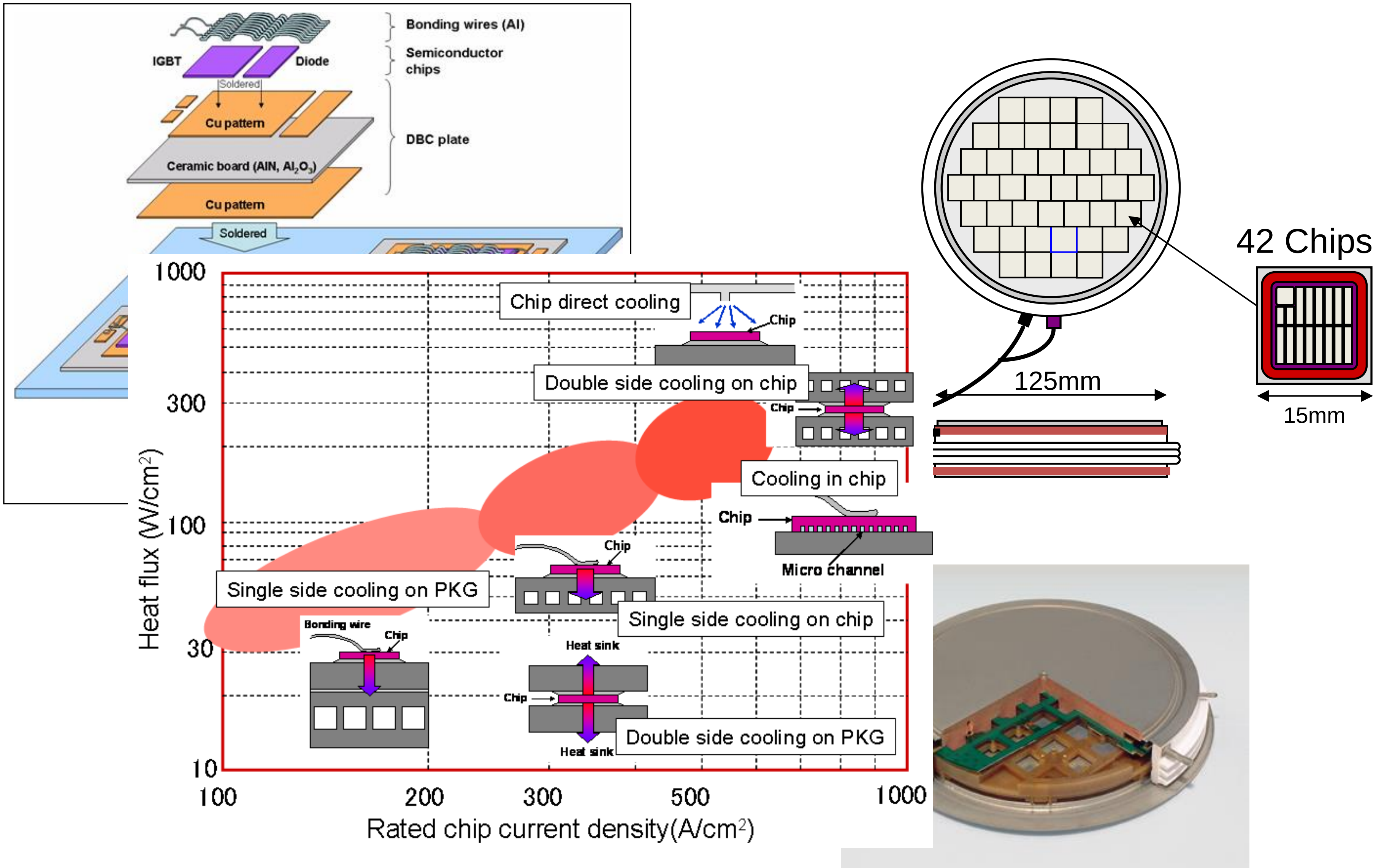
Future possibility

- **1) Si-power devices still have much room for development toward ultimate MOSFETs and IGBTs.**
- **2) The combination of Si-switching devices and SiC freewheeling diodes will be a significant step not only for strengthening the SiC market but also for Si-device development.**
- **3) Si-IGBT will be replaced by SiC MOSFET in the voltage range of more than 1000 V in some applications, and SiC-IGBT has the potential to be used for applications of more than 10 kV. (Si-IGBT for volume market, SiC for high end market)**
- **4) GaN power devices will replace some of Si-power ICs and will be used for faster switching applications.**
- **5) The unique properties of diamond have potential for new power devices particularly in high-voltage applications.**
- **6) The ultimate CMOS has the potential to be used for power integrated devices in ICT applications.**

H Ohashi, I Omura - IEEE transactions on electron devices, 2013

Related Technology

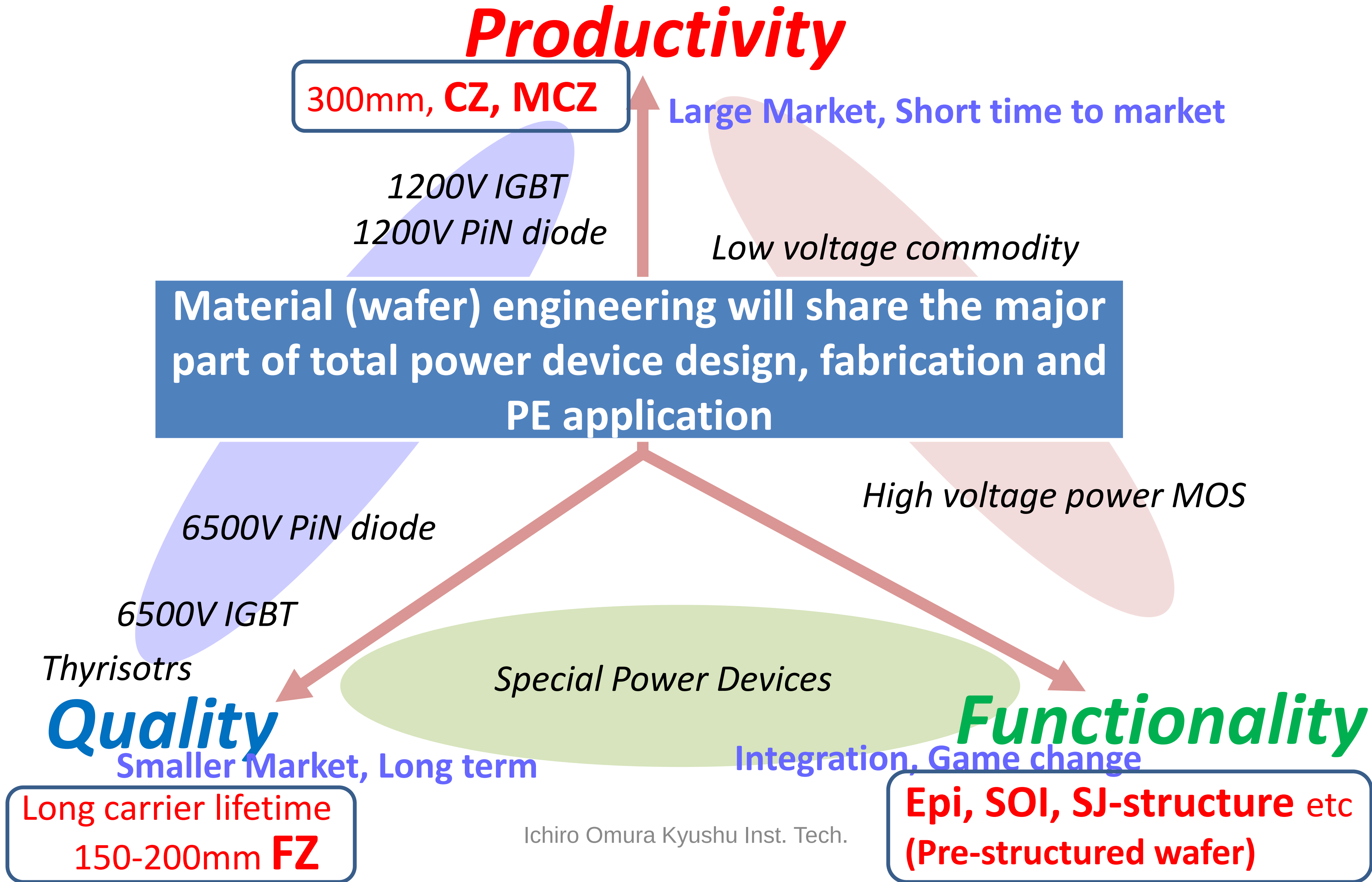
Examples of High Power IGBT Package



Ichiro Omura Kyushu Inst. Tech.

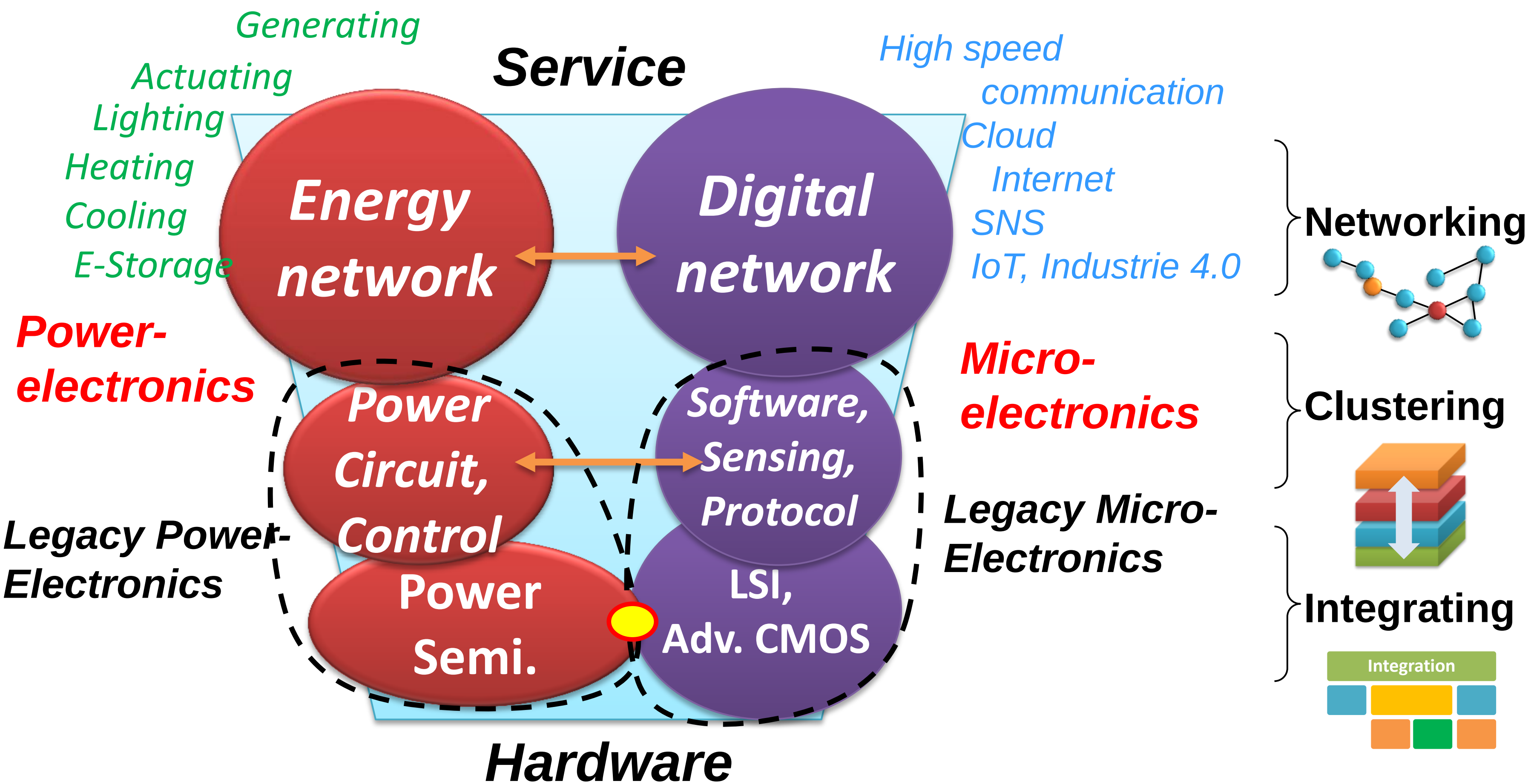
Shen, Omura, “Power Semiconductor Devices for Hybrid, Electric, and Fuel Cell Vehicles” Proc. Of the IEEE, Issue 4, 2007

Wafer technology(Silicon)



Power electronics and micro electronics

forming Cyber-Physical System



- **Electron devices are the key technology for future energy networking**
- **New phase of electronics has started with close link between power and micro electronics for future sustainable society**

I. Omura, SIIQ report, Oct. 2012, in Japanese

See also

Z. John Shen, Ichiro Omura
Article Power Semiconductor Devices for Hybrid, Electric, and Fuel Cell Vehicles
Proceedings of the IEEE 05/2007; 95(4-95):778 - 789.

H. Ohashi and I. Omura “Role of Simulation Technology for the Progress in Power Devices and Their Applications,” IEEE T-ED, Vol. 60, issue 2, 2013.