Novel Trench Power MOSFETs and Structure-based Compact Model for High Efficiency Electronics Application

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高効率エレクトロニクス応用のための新構造トレンチパワーMOSFET と素子構造に基づいたコンパクトモデルの開発

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ABSTRACT

Actions for sustainable society realization, that is a global climate change mitigation and related energy problem solutions, are being executed in various fields. It is publicly said that it is necessary to reduce emissions of a carbon dioxide (CO_2) to approximately 50% of the present level by 2050. Among various measures for accomplishment of the scenario, an improvement effect by the contribution of power electronics is greatly expected, as an electric energy sector. A power semiconductor device is a fundamental device underpinning the power electronics technology. The power semiconductor devices are widely used in many applications, and the device performance is being improved continually to get the high efficiency. In a category of low-voltage (10–250 V) and high-frequency (10 kHz–1 MHz) operation, silicon power MOSFETs (Metal Oxide Field Effect Transistors) are widely used. For the market demand for low power loss and high efficiency, the power MOSFETs' research and development in many aspects including a device structure, a manufacturing process, and a packaging technology are performed continuously. In this study, novel structures to achieve the low-power-loss MOSFET were proposed and experimented. In addition, structure-based compact models to enable the power loss calculation were newly constructed.

In chapter 1, performance requirements for the power MOSFETs were revealed, and the elements which decide the power loss in an application circuit were classified. Challenges for the low power loss in the low-voltage devices and directions for the novel structure development were described. In addition to a conduction loss improvement that comes from an on-resistance ($R_{ON}A$) reduction with a necessary breakdown voltage maintained, it was pointed out that the electric charge accumulated to an output capacitance, which affects to a switching loss, was significant issue particularly in high-speed switching. In the low-power-loss structure design, it was described that the construction of the capacitance model is very important as well as the $R_{ON}A$ model.

In chapter 2, in a planar gate double-diffused MOSFET (D-MOSFET) and a trench gate MOSFET (U-MOSFET), the basic structures and the $R_{ON}A$ components were described. The conventional $R_{ON}A$ models were analyzed, restructured, classified, and compared with developed devices. Moreover, the device performance limit was indicated.

In chapter 3, in a superjunction U-MOSFET (SJ-UMOSFET) and a field-plate U-MOSFET (FP-MOSFET) which are evolution structure of the U-MOSFET, the basic structures, the basic principles, and the $R_{ON}A$ components were described. The conventional $R_{ON}A$ models were analyzed, restructured, newly classified, and compared with developed devices. Moreover, the device performance limit was indicated.

In chapter 4, components of the parasitic capacitances that are important to the switching loss design of the low-voltage MOSFET were clarified. For the latest slant FP-MOSFET that structure was complicated, model equations of output capacitance (C_{oss}) and reverse transfer capacitance (C_{rss}) were constructed based on the device structural parameters.

In chapter 5, a validity of the model that derived in chapter 4 was verified. Drain voltage dependences of C_{oss} and C_{rss}, for 100-V-class D-MOSFET and slant FP-MOSFET, were analyzed. An accuracy of the model was identified using simulation results of TCAD (Technology Computer Aided Design). In addition, each component for the switching loss analysis was derived from the constructed capacitance model.

In chapter 6, the power loss analysis of the slant FP-MOSFET was carried out based on the models described in previous chapters, and the results were compared with the conventional device. It was revealed that the performance of the slant FP-MOSFET was superior in high-frequency use. In addition, by adopting a gate connection field-plate structure, it was found that the high efficiency is achieved in low-frequency and high-current use.

In chapter 7, by utilizing the $R_{ON}A$ models and the capacitance models of the slant FP-MOSFET, the device performance limit was pursued. As a result, it became clear that the efficiency for the high-frequency switching application can be improved by over 50% and that for the low-frequency and high-current application can be improved by over 70%.

In chapter 8, as conclusion, the proposal of the novel FP-MOSFET structure, the construction of the compact model, and the possibility of the device performance improvement that is greater than 50% were described.

This dissertation describes, for the low-power-loss MOSFET that is key device to prevent the CO_2 emission, the construction of the device physics based compact model, which can design in short term without experiment and simulation. This indicates a guiding principle of the future low-power-loss MOSFET design by the compact model for the first time. By applying the proposed compact model, it becomes clear that the FP-MOSFET structure has an enough room for the performance improvement and this device should advance the research and development. It is expected this compact model can greatly contribute to higher efficiency power electronics.

日本語概要

地球規模の気候変動抑制やエネルギー問題への対応など、持続可能社会の実現に向けての取り組みが様々な分野で行われており、2050 年までに二酸化炭素排出量を現状レベルの約 50%まで削減する必要があると公的に言われている。この目標達成に向けた施策の中で、電気エネルギーのセクターでは、パワーエレクトロニクスの貢献による効率改善効果が大きく期待されている。パワーエレクトロニクス技術を支える基幹デバイスがパワー半導体デバイスである。パワー半導体デバイスは広範囲なシステムや機器に使用されおり、高効率化に向けてデバイス性能改善が継続的に行われている。パワー半導体デバイスの中でも低電圧(数 10V～250V)、高周波数動作(数 10kHz～1MHz)のカテゴリでは、パワーMOSFET(金属酸化膜電界効果トランジスタ)が広く使用されており、低損失・高効率化に向けて、デバイス構造、製造プロセス、実装技術など多方面での研究が行われている。本研究では、パワーMOSFET の低損失化を実現する新デバイス構造を提案し、試作を行うとともに、損失計算を可能とする新しいコンパクトモデルを構築した。

本論文の 1 章では、パワーMOSFET への要求性能を明らかにし、想定する応用回路において損失を決定する要素を分類、低耐圧デバイスの低損失化に必要な課題を明らかにし、新構造開発に向けての指針を示した。また、必要な耐圧を維持しつつオン抵抗を改善する導通損失の低減に加え、スイッチング損失の中でも特に出力容量に蓄積する電荷が高速動作時の課題になることを指摘し、オン抵抗モデルだけでなく容量モデルの構築が低損失化において重要であることを示した。

2 章では、プレーナゲート二重拡散 MOSFET(D-MOSFET)およびトレンチゲート MOSFET(U-MOSFET)の基本構造とオン抵抗の構成要素を述べ、従来のオン抵抗モデルを解析、再構成、分類するとともに試作デバイスと比較し、その限界を明らかにした。

3 章では、U-MOSFET の進化構造であるスーパージャンクション MOSFET(SJ-UMOSFET)とフィールドプレート MOSFET(FP-MOSFET)の基本構造と基本原理、オン抵抗の構成要素を述べ、従来のオン抵抗モデルを解析、再構成、分類するとともに試作デバイスと比較し、その限界を明らかにした。

4 章では、低耐圧 MOSFET のスイッチング損失設計に重要な寄生容量の構成要素を明らかにし、構造が複雑な最新の傾斜 FP-MOSFET について、デバイス構造パラメータをもとにした出力容量(C_{oss})と帰還容量(C_{rss})のモデル式を構築した。

5 章では、4 章で導出したモデルの妥当性を検証した。100V クラスの D-MOSFET と傾斜 FP-MOSFET について Coss、Crss のドレイン電圧依存性を解析し、TCAD(Technology Computer Aided Design)によるシミュレーション結果を用いてモデルの精度を確認した。また、構築した容量モデルからスイッチング損失解析のための各要素を導出した。

6 章では、前章のモデルをもとに傾斜 FP-MOSFET の解析を行い、従来デバイスと比較した。高周波では FP-MOSFET が優位であり、また低周波・大電流用途ではゲート接続型の FP 構造を採用することで高効率化が可能であることを明らかにした。

7 章では、傾斜 FP-MOSFET 構造のオン抵抗モデルと容量モデルを活用し、性能限界を追求した。その結果、高周波スイッチング用途で 50%、低周波スイッチング用途で 70%の効率改善が可能であることが判明した。

8 章では、本論文の結論として、新しい FP-MOSFET 構造の提案とコンパクトモデルの構築、さらに今後 50%以上の性能向上が可能であることを述べた。

本論文は、二酸化炭素排出量の抑制に対してキーデバイスとなるパワーMOSFET の低損失化に向け、試作やシミュレーション等を行うことなく短期間で設計可能なデバイス物理に基づくコンパクトモデルの構築、そしてコンパクトモデルによる今後の低損失化設計の指導原理を初めて示したものである。本提案のコンパクトモデル適用により、FP-MOSFET 構造での性能改善余地が十分あること、研究・開発を推進すべきデバイスであることが明らかになり、パワーエレクトロニクスの更なる高効率化に大いに貢献できることが期待される。

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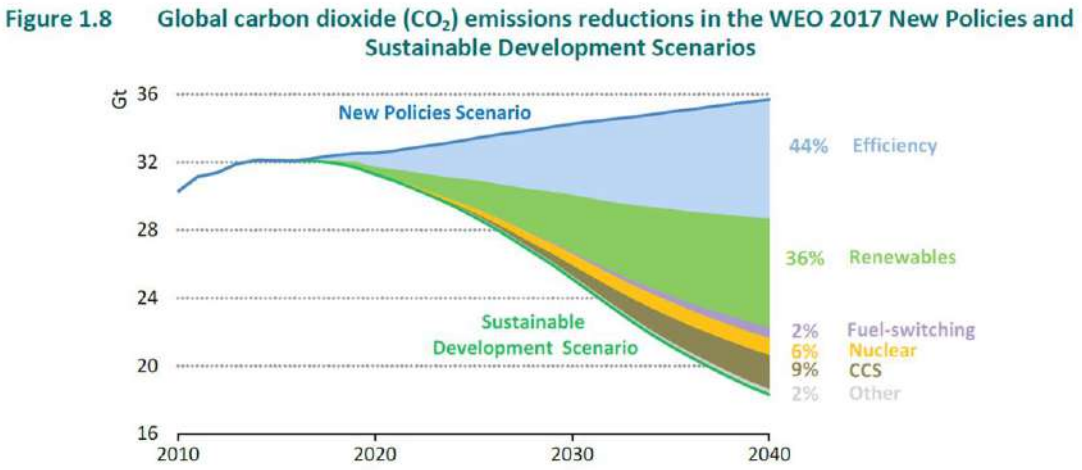
Prof. Satoshi Matsumoto
Co-advisor Prof. Mengu Cho
Prof. Kazuhiro Toyoda

1. BACKGROUND AND OBJECTIVE

1.1. Overview of power electronics in our society and role of power semiconductor devices

Actions for sustainable society realization, that is a global climate change mitigation and related energy problem solutions, are being executed in various fields. To suppress a temperature rise after the Industrial Revolution to less than 2 degrees Celsius is the particularly important numerical target, which was concluded in Paris agreement (December 2015). In order to achieve the target, it is said that it is necessary to reduce a carbon dioxide (CO_2) emissions to approximately 50% of the present level by 2050. An improvement effect by the contribution of power electronics is greatly expected in a measure for the scenario accomplishment.

The World Energy Outlook (WEO) 2017 has shown that an efficiency will realize over 40% of the CO_2 emissions reductions, among the combination of other measures [1]. It means the contribution of an energy use efficiency in various electronics system will be larger rather than increasing the supply of renewable energy, as shown in Fig. 1-1 [2].



Source: IEA (2018) Energy efficiency 2018. All rights reserved.

Fig. 1-1. Global carbon dioxide (CO_2) emissions reductions in *the World Energy Outlook* (WEO) 2017 [1] New Policies and Sustainable Development Scenarios. [2]

A key device supporting this power electronics technology is a power semiconductor device. The power semiconductor devices are used to a great variety of: the large-scale application such as a power generation, a power transmission and distribution, and a train system; medium and small-size application such as an industrial equipment, a car, a home electric appliance, a mobile device (Fig. 1-2).

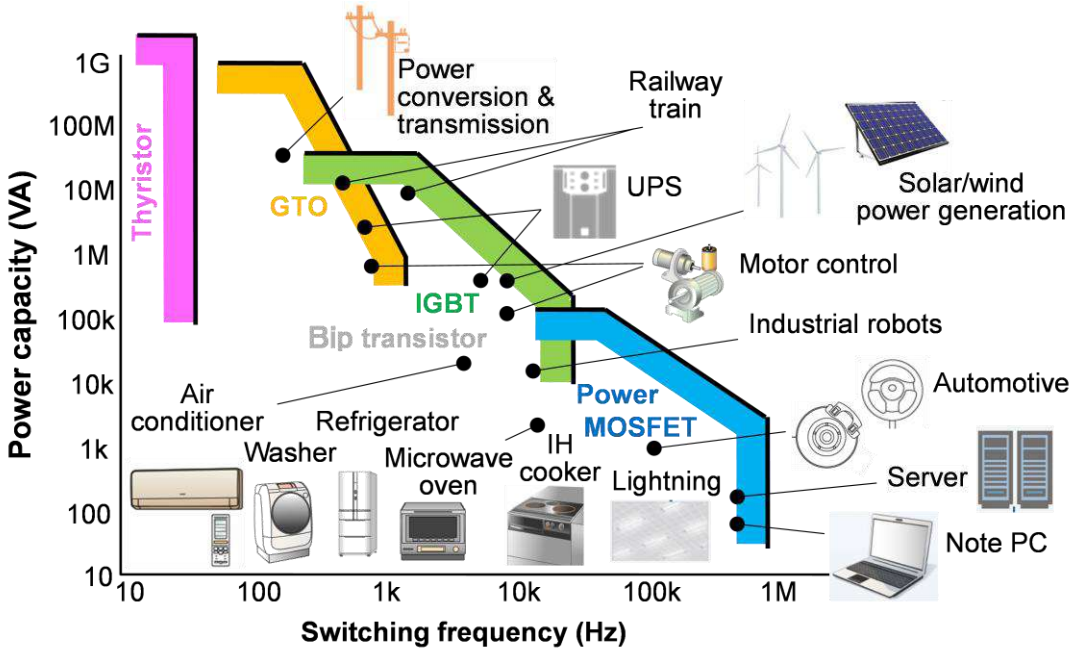
There are several kinds of power semiconductor devices, and those are selected corresponding to a power capacity and a switching frequency as follows.

Power MOSFET (Metal Oxide Field Effect Transistor): low power, medium to high frequency.

IGBT (Insulated Gate Bipolar Transistor): medium to high power, low to medium frequency.

GTO (Gate Turn-Off Thyristor): high power, low frequency.

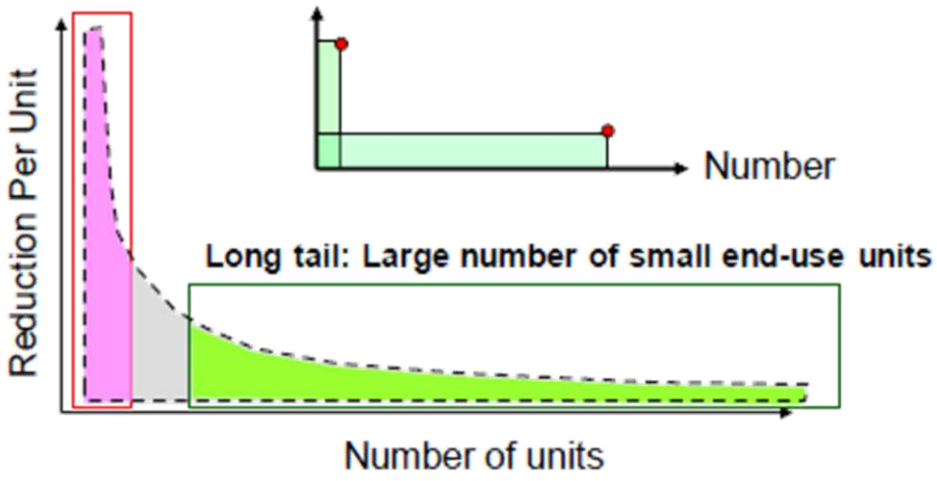
Thyristor: high to ultra-high power, low frequency.



Source of illustrations: Renesas Electronics Corporation, http://www.renesas.com/jp/ja/

Fig. 1-2. Power semiconductor devices application map.

The power semiconductor devices are contributing to the reduction of energy consumption in many applications from very small portable devices to very large-scale power electronics systems. In other words, the power semiconductor devices have big responsibilities to the CO_2 emission reductions in each category of the electronics system/unit/equipment. This image can be shown in Fig. 1-3 [3] [4]. Although the CO_2 reduction rate per unit is very high in the large-scale application such as the power plant, the contribution is restrictive. On the other hand, large number of small end-use units has big contribution that cannot be ignored at all.

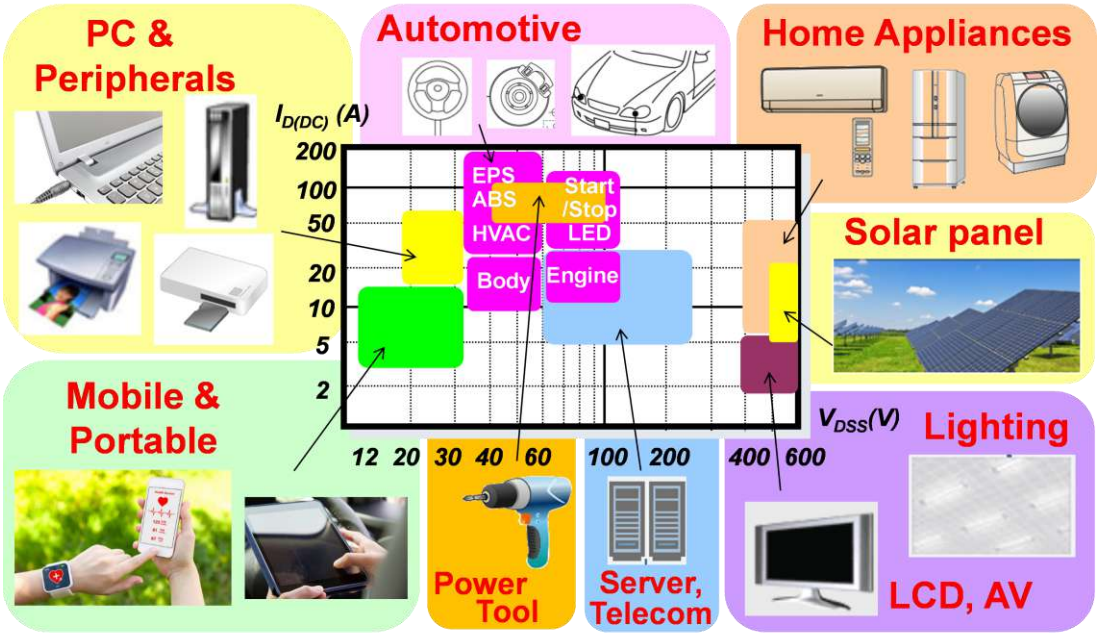


From "Scaling up demand-side energy efficiency improvements through programmatic CDM" *Energy Sector Management Assistance Program and The World Bank Carbon Finance Unit*, p. 8, 2007, [3] (modified).

Fig. 1-3. Schematics of volume of the CO_2 emission reductions in each category of the electronics system/unit/equipment. [4]

1.2. Applications and market demands for power MOSFETs

In the power semiconductor device which is categorized into low-voltage (12–250 V) and high frequency (10 kHz–1 MHz) application, silicon power MOSFET is used in so many applications: e.g., mobile and portable equipment, personal computers and peripheral devices, automotive electronics units, power tools, high-end servers for data center and other facilities, home appliances, lightning equipment, audio and visual equipment, photovoltaic inverter on solar panel, and so on. Fig. 1-4 is the power MOSFETs application map shown in the matrix of the rated-voltage (V_{DSS}) and the rated-current ($I_{D(DC)}$). From a viewpoint of the industry, the power MOSFET is a business field having a big market of approximately 7000 million dollars.



Source of illustrations: Renesas Electronics Corporation, http://www.renesas.com/jp/ja/

Fig. 1-4. Power MOSFETs application map.

For various market demands such as low cost, high productivity, small size, light weight, high efficiency, low power consumption, high power rating, stability, and safety operation, the power MOSFETs' research and development (R&D) in many aspects including a material, a manufacturing process, a device structure, a package, a packaging method, a reliability technology, a design technology, and a measurement technology are performed continuously (Fig. 1-5).

As the device performance that contributes directly to high efficiency and low power consumption of the application, a low-power-loss technology of the power MOSFET is very important. Therefore, a new structure, a new process, a design technique, and an evaluation technique, which can embody the low power loss, are strongly demanded and that is responsibilities for the R&D.

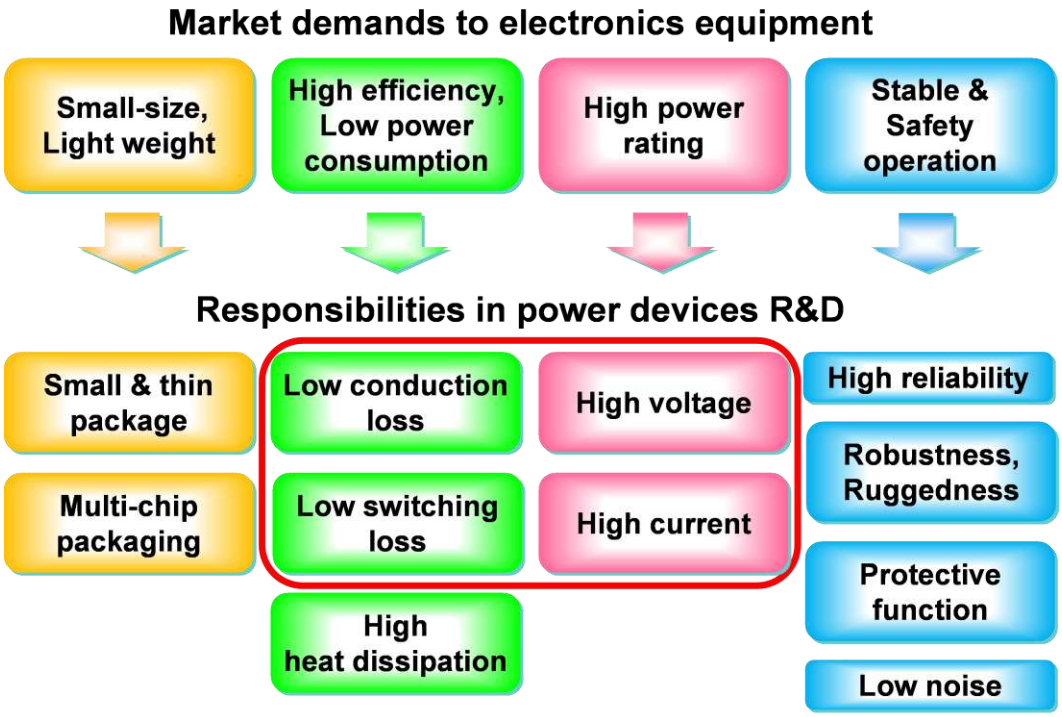


Fig. 1-5. Market demands to electronics equipment and responsibilities as power devices R&D.

1.3. Classification of power MOSFETs

The power MOSFETs are classified into two rated-voltage ranges: 12–250 V as low-voltage (LV) and 400–800 V as high-voltage (HV). Historically, planar gate double-diffused MOSFETs (D-MOSFETs) [5] [6] and trench gate MOSFETs (U-MOSFETs) [7] were developed in the 1970s–1980s, respectively, and they are currently used as matured low-cost devices. As great advancement of the power MOSFETs in terms of performance, field-plate trench MOSFETs (FP-MOSFETs) [8], superjunction MOSFETs (SJ-MOSFETs) [9], and superjunction U-MOSFETs (SJ-UMOSFETs) [10] were devised in the 1990s–2000s. The development history and the device structure are described in sections 2.1 and 3.1.

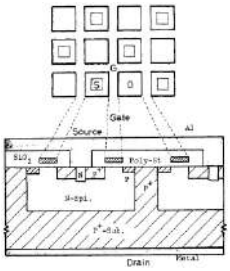
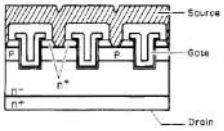
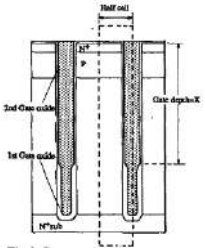
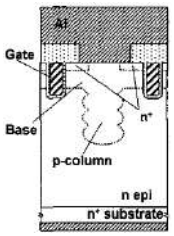
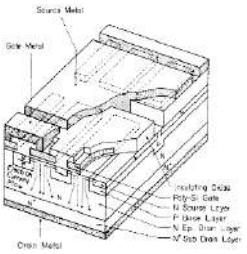
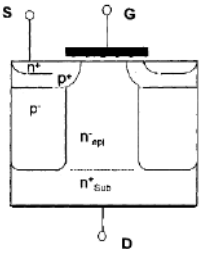
	D-MOSFET	U-MOSFET	FP-MOSFET	SJ-UMOSFET
Low-voltage 12–250V	[5] © 1975 IEEE 	[7] © 1985 IEEE 	[8] © 1992 IEEE 	[10] © 2004 IEEE 
High-voltage 400–800V	D-MOSFET [6] Copyright 1982, The Japan Society of Applied Physics 			SJ-MOSFET [9] © 1997 IEEE 

Fig. 1-6. Classification of power MOSFETs. Rows show range of rated-voltage, and columns show cell structures which has been proposed in each early development stage.

1.4. Challenges on power MOSFETs for the low-voltage application

1.4.1. Necessity of improving tradeoff characteristics

As mentioned the above (Fig. 1-5), market demands for the power MOSFETs are including many different things. There is various tradeoff relationship each other, between device performances, device size, ease of use, manufacturing cost, productivity, and so on. To overcome the various tradeoff and to provide advanced high performance products are big challenge in power MOSFET development.

In all power MOSFETs dealing with high current, an on-resistance (R_{ON}) reduction to minimize the power loss and a high breakdown voltage (V_B) maintaining are fundamental tradeoff. The R_{ON} is mainly occupied by drift layer length and the impurity concentration, which also determine the V_B. The R_{ON} is derived by [11] and expressed as below.

$$R_{ON} \approx \frac{4{V_B}^2}{\mu_n \varepsilon {E_C}^3} \tag{1-1}$$

Here, μ_n is the electron mobility, ε is the permittivity of semiconductor, and E_C is the critical electric field. The higher the V_B is, the more the R_{ON} increases, therefore the R_{ON}–V_B tradeoff is a still significant issue on the power MOSFETs development.

The power MOSFET has parasitic capacitances itself: gate–source capacitance (C_{gs}), gate–drain capacitance (C_{gd}), and drain–source capacitance (C_{ds}). The parasitic capacitances affect to switching loss. There is a simple tradeoff between the chip size and the capacitances; the larger the chip size, the more the capacitances increase. In addition, in unit cell structure of the power MOSFET, there are various cases that a reduction method of the capacitance affects to the V_B increase or the R_{ON} increase. Thus, to make sure of the relationship between the R_{ON} and the capacitance properties, figures-of-merit (FOMs) are discussed, especially in considering a switching performance.

1.4.2. Minimization of power loss to improve energy use efficiency

The LV-MOSFETs, which are generally classified into rated-voltage in the range from 12–250 V, are applied in various power electronics circuits, e.g., as shown in Fig. 1-7, Fig. 1-8, and Fig. 1-9.

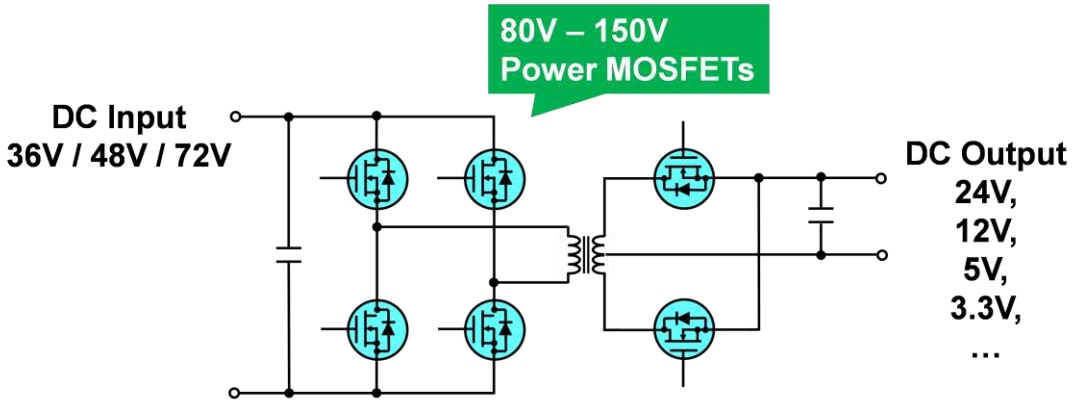


Fig. 1-7. Example of application circuit topology (1). Isolated DC-DC converter block having full bridge for primary-side and synchronous rectification for secondary-side.

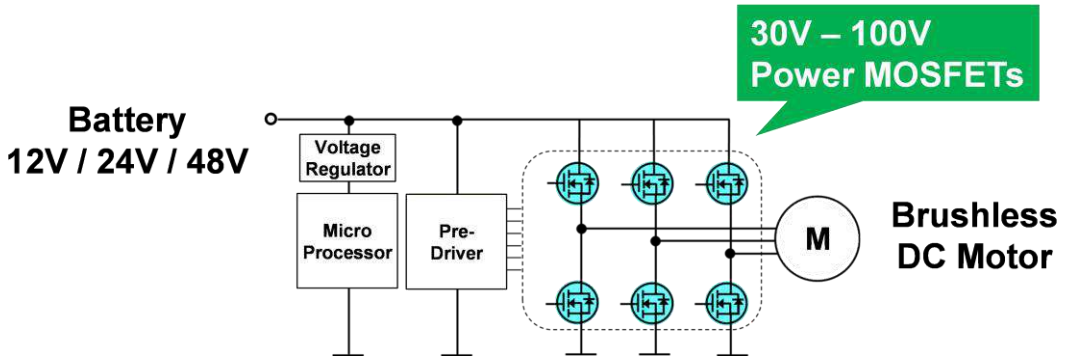


Fig. 1-8. Example of application circuit topology (2). Motor drive unit having three-phase inverter.

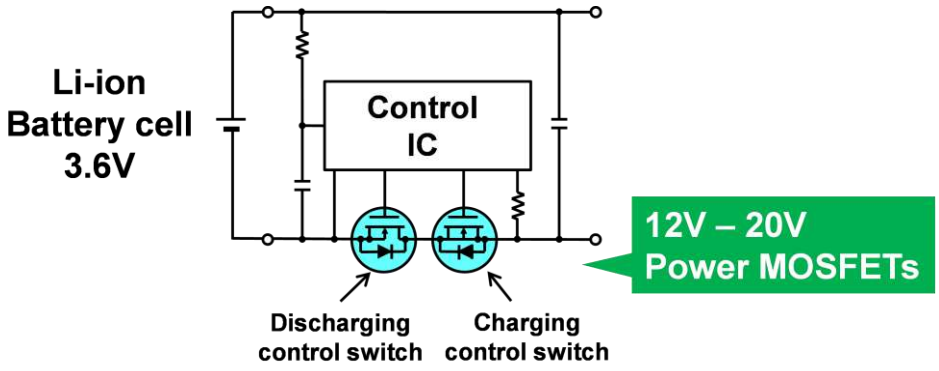


Fig. 1-9. Example of application circuit topology (3). Lithium-ion battery cell charging/discharging control and protection circuit.

In the distributed power supply systems, there is an isolated DC-DC converter block having full bridge for primary-side and synchronous rectification for secondary-side, as shown in Fig. 1-7. Corresponding to the DC input voltage, 80–150-V-rated power MOSFETs are used in both primary-side and secondary-side. When the DC output voltage is set to 12 V, a 30-V-rated power MOSFET is used in the next stage.

In the motor drive unit as shown in Fig. 1-8, three-phase inverter circuit is consists of six power MOSFETs. For example, in the automobile electronic unit, corresponding to the battery voltage, 30–100-V-rated power MOSFETs are used in the inverter circuit.

In the lithium-ion battery pack, which is incorporated in large quantities in many kinds of portable equipment, 12–20-V-rated power MOSFETs are used in the battery cell charging/discharging control and protection circuit (Fig. 1-9).

In such an energy conversion, a load drive, or a switching operation, an energy loss is caused generally. In a switching circuit using the power MOSFET as shown in Fig. 1-10, the power loss occurs during both conduction and switching period. The general power loss consists of the following components [12] [13].

P_{GD}	Gate drive loss
P_{CON}	Conduction loss
$P_{SW(on)}$	Turn-on loss
$P_{SW(off)}$	Turn-off loss
P_{Qrr}	Diode reverse recovery charge (Q_{rr}) loss
P_{Qoss}	Output charge (Q_{oss}) loss

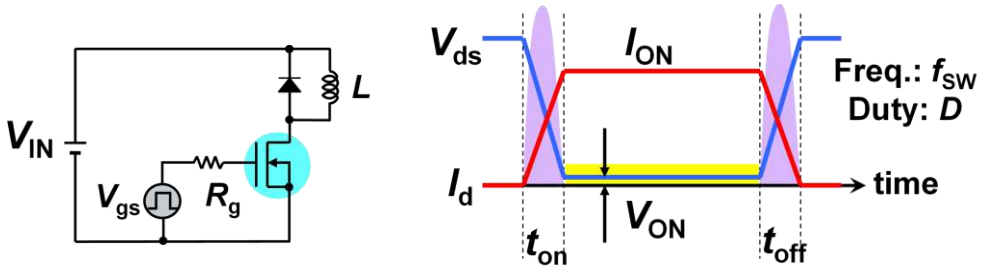


Fig. 1-10. Simplified switching test circuit (left figure) and switching waveform (right figure).

V_{IN}: input (supply) voltage, V_{gs}: gate voltage, R_g: gate resistance, L: inductance, V_{ds}: drain–source voltage, I_d: drain current, I_{ON}: on-state current, V_{ON}: on-state voltage, t_{on}: turn-on switching time, t_{off}: turn-off switching time, f_{SW}: switching frequency, and D: duty ratio.

Components of power loss originated from the power MOSFET characteristics in an assumption of the switching test circuit in Fig. 1-10 and formula of each power loss are shown in Fig. 1-11. In each power loss component, individual improvement methods are considered as described below.

P_{GD} reduction is depending on a gate driver technology. It is expected that P_{GD} can be minimized by very low impedance condition and very high current gate drive [14] [15] [16].

P_{CON} is proportional to the R_{ON}. Ultralow R_{ON} MOSFET can directly reduce P_{CON}.

$P_{SW(on)}$ and $P_{SW(off)}$ increase in proportion to the switching time (turn-on switching time (t_{on}) and turn-off switching time (t_{off})) and the switching frequency (f_{SW}). Meanwhile, t_{on} and t_{off} are defined by both gate–source capacitance (C_{gs}) and gate–drain capacitance (C_{gd}). Low gate–source charge (Q_{gs}) and low gate–drain charge (Q_{gd}) MOSFET is the most desirable solution. Both $P_{SW(on)}$ and $P_{SW(off)}$ can be also minimized by very low impedance condition and very high current gate drive. Moreover, in particular, $P_{SW(on)}$ can be drastically reduced by a circuit control technology such as zero-voltage-switching (ZVS)

P_{Qrr} is defined by the reverse recovery charge (Q_{rr}) of body diode, which is formed by pn-junction of the MOSFET. Low-recovery-charge Shottky barrier diodes (SBD) can improve P_{Qrr} drastically.

P_{Qoss} is caused by the period of output charge (Q_{oss}) charging and discharging by drain current (I_d). Q_{oss} is influenced by drift layer design that determines the V_B.

Regarding advanced power MOSFETs, it is obvious that there is a potential to reduce P_{CON}, $P_{SW(on)}$, and $P_{SW(off)}$ drastically, and several power loss analysis has been reported so far [17] [18] [19] [20] [21] [22] [23]. However, owing to the V_B maintained structure, the Q_{oss} increase which leads to P_{Qoss} is a significant issue, especially in the case of megahertz switching.

Power loss	Formula	Improvement method
Gate drive	$P_{GD} = Q_g V_{gs} f_{SW}$	Low gate impedance (R_g~0) and high current drive by **gate driver technology**
Conduction	$P_{Con} = {I_{ON}}^2 R_{ON} D$	**Ultra low R_{ON}** MOSFET
Turn-on	$P_{SW(on)} = \frac{1}{2} V_{ds} I_d t_{on} f_{SW}$	**Low Q_{gs} and Q_{gd}** MOSFET Low gate impedance (R_g~0) and high current charging/discharging by **circuit control technology**
Turn-off	$P_{SW(off)} = \frac{1}{2} V_{ds} I_d t_{off} f_{SW}$	
Diode recovery	$P_{Qrr} = Q_{rr} V_{IN} f_{SW}$	**Low Q_{rr}** (recovery charge) SBD
Output charge	$P_{Qoss} = f_{SW} \int C_{oss} V_{ds} dV$	**To reduce C_{oss} charging / discharging**

Fig. 1-11. Components of power loss originated from the power MOSFET characteristics in an assumption of the switching test circuit in Fig. 1-10. Each power loss is expressed by general formula. In addition, improvement methods for each power loss are described.

V_{IN}: input (supply) voltage, V_{gs}: gate voltage, R_g: gate resistance, Q_g: gate charge, V_{ds}: drain–source voltage, I_d: drain current, I_{ON}: on-state current, t_{on}: turn-on switching time, t_{off}: turn-off switching time, f_{SW}: switching frequency, D: duty ratio, Q_{rr}: reverse recovery charge, Q_{gs}: gate–source charge, Q_{gd}: gate–drain charge, and C_{oss}: .output capacitance.

1.5. Objective of this study

1. Development of novel structures for low-voltage power MOSFETs to achieve low power loss.
2. Construction of structure-based compact model to enable the power loss analysis.
3. Proposal of an ultimate power MOSFET structure by using the compact model and prediction of the performance.

For the key device to prevent the CO_2 emission, low-power-loss technologies of the power MOSFETs are strongly required to realize high efficiency and low power consumption in various application. In this dissertation, several kinds of new structures for the low-power-loss LV-MOSFETs are proposed and are demonstrated with fabricated devices.

In addition, to enable a new device design without experiment and simulation, a device-physics-based compact model for the LV-MOSFET are constructed. It is expected that the compact model can calculate and predict significant number of the new designed devices in very short term. Fig. 1-12 shows schematics of procedure from the device structure design to the device performance evaluation/prediction, for the case of a real device, a TACD simulation, and a calculation by using the compact model.

As the compact model, specific on-resistance ($R_{ON}A$) models, which are necessary for the calculation of the conduction loss, are described in detail for each LV-MOSFET structure. It needs to be considered carefully that not only the $R_{ON}A$ components in each structure but also the current spreading in vertical direction will change by the structure design or the layout design.

Moreover, especially in high current or high frequency switching application, parasitic capacitances in the LV-MOSFET are necessary for the calculation of the switching loss. The capacitance models are described by structural parameters, which are unit-cell geometries, impurity doping concentration, and dimensions of the device structure. In the modeling, the components of capacitance for both standard D-MOSFETs and the latest FP-MOSFETs are considered and the derivation of model equations is studied in detail.

By utilizing the compact model, it enables to predict an ultimate structure for next-generation LV-MOSFET. It makes clear that the latest FP-MOSFET structure has an enough room for the performance improvement and the device should advance the research and development. It is expected this compact model can greatly contribute to higher efficiency power electronics.

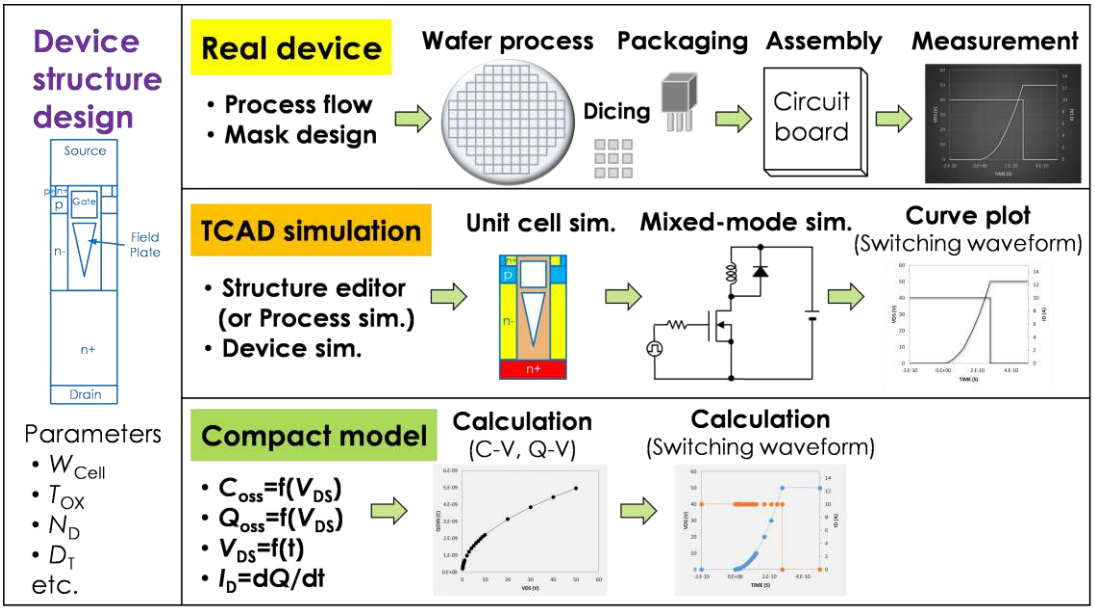


Fig. 1-12. Schematics of procedure from device structure design to device performance evaluation/prediction: for real device, TACD simulation, and compact model.

2. Development of Advanced Low Power Loss D-MOSFETs and U-MOSFETs

2.1. Earlier studies in LV-MOSFETs Development

For the most basic structure of modern power MOSFETs, which drain current flows vertically between front-surface and back-surface in semiconductor die, planar gate double-diffused MOSFETs (D-MOSFETs) were developed in the mid-1970s [5] and commercialized in the late 1970s. The D-MOSFETs applied fundamental technology called Diffusion Self-Aligned (DSA), which was devised in the late 1960s [24].

Trench D-MOSFETs were developed in the mid-1980s [7] and commercialized in the early 1990s, respectively. The trench gate D-MOSFETs which have U-grooved structure, are also called U-MOSFETs, and currently being used as matured low-cost devices. As great advancements of LV-MOSFETs in terms of performance, field-plate U-MOSFETs (FP-MOSFETs) and superjunction U-MOSFETs (SJ-UMOSFETs) were developed and commercialized in the early to mid-2000s. Regarding SJ-UMOSFETs and FP-MOSFETs, the details are described in chapter 3.

Fig. 2-1 shows technology development history of vertical power MOSFETs.

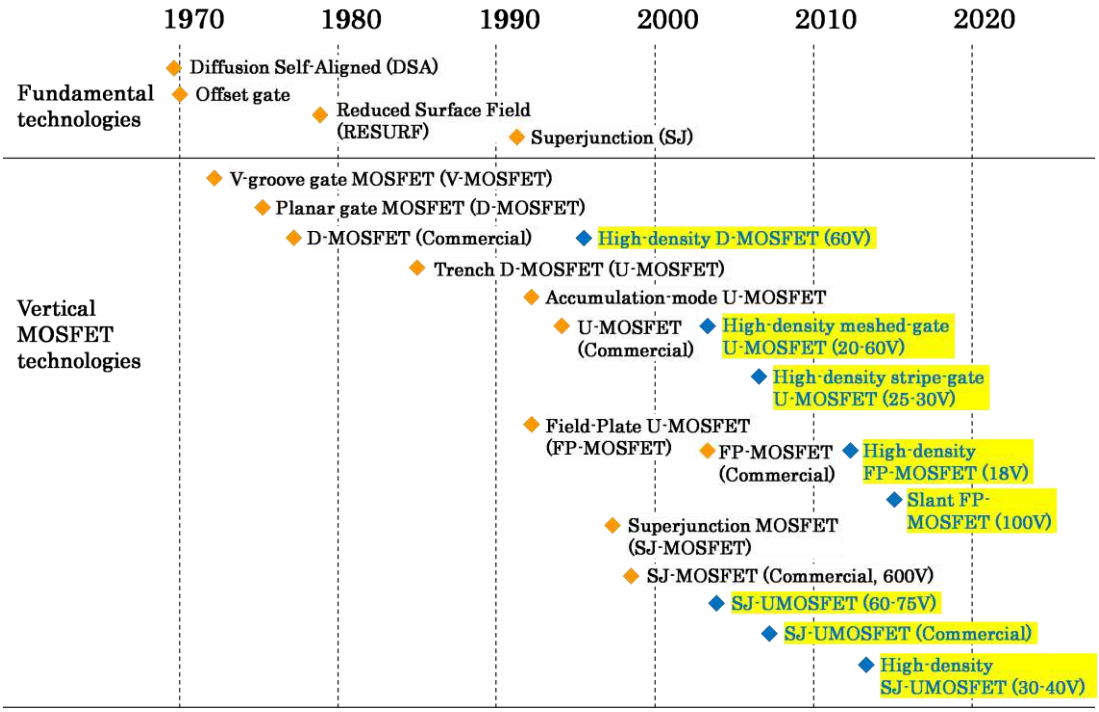


Fig. 2-1. Technology development history for vertical power MOSFETs. Highlights show author's research.

2.2. Improvement of planar gate double-diffused MOSFET (D-MOSFET)

2.2.1. Basic structure and on-resistance ($R_{ON}A$) components of D-MOSFET

Schematic cross-sectional unit-cell structure of D-MOSFET is shown in Fig. 2-2. Fig. 2-2(a) shows a distribution of electric field E_y of drift layer in vertical direction y, when reverse bias applies to drain. In the D-MOSFET, breakdown voltage (V_B) of one-dimensional plane pn-junction is determined by the area of this triangle electric field. When a gate width is relatively short, i.e., a lateral distance between p–base layers is narrow enough, the V_B of the D-MOSFET is approximated as

$$V_B \approx \frac{1}{2} E_C L_{dep}, \tag{2-2}$$

where E_C is a critical electric field and L_{dep} is a depletion layer length in y. In an assumption, if a depletion layer length in the p–base region is negligible a slope of the electric field in the n–drift layer is expressed as

$$\frac{E_C}{L_{dep}} = -\frac{qN_D}{\varepsilon_{Si}\varepsilon_0}, \tag{2-3}$$

where q is the elementary charge, N_D is the n–drift layer concentration, and $\varepsilon_{Si}\varepsilon_0$ is the permittivity of silicon. By substituting Eq. (2-3) into Eq. (2-2), the V_B can be obtained as

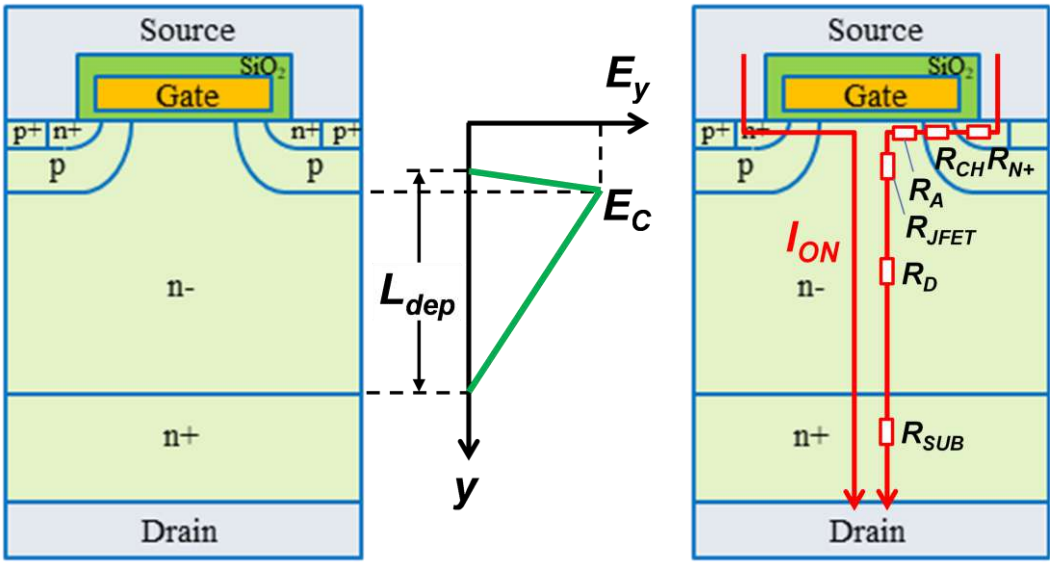
$$V_B \approx \frac{\varepsilon_{Si}\varepsilon_0 {E_C}^2}{2qN_D}. \tag{2-4}$$

The V_B is inversely proportional to the N_D. On the other hand, the N_D is one of the main influence parameter of on-resistance ($R_{ON}A$), especially in drift layer resistance (R_DA) as described below. Therefore, the V_B and the R_DA has a tradeoff relationship, and it has been described as $R_DA \propto V_B^{2.5}$ in [11].

Fig. 2-2(b) shows on-state current paths and on-resistance components of the D-MOSFET. The $R_{ON}A$ of the D-MOSFET ($R_{ON}{}^{DMOS}A$) is described as follows.

$$R_{ON}{}^{DMOS}\mathrm{A} \cong R_{N+}A + R_{CH}A + R_AA + R_{JFET}A + R_DA + R_{SUB}A \tag{2-5}$$

Here, R_{N+} is n^+–source layer resistance, R_{CH} is channel resistance, R_A is accumulation layer resistance under the gate, R_{JFET} is junction FET (JFET) resistance, R_D is n–drift



(a) (b)

Fig. 2-2. Schematic cross-sectional structure of D-MOSFET, which shows unit-cell area. (a) Electric field distribution in vertical direction of off-state. (b) On-state current paths and components of on-resistance.

layer resistance and R_{SUB} is n^+–substrate resistance. All the components indicate the resistance of unit area "A", which means the product of "unit width" and "unit length". Whereas $R_{N+}A$ is relatively small, thus $R_{ON}{}^{DMOS}A$ can be approximated by using main components,

$$R_{ON}{}^{DMOS}\mathrm{A} \approx R_{CH}A + R_AA + R_{JFET}A + R_DA + R_{SUB}A. \tag{2-6}$$

In Eq. (2-6), each of the resistance except R_DA is expressed by analytical model as below [25] [26] [27].

$$R_{CH}\mathrm{A} = \frac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}(V_{gs} - V_{TH})} \tag{2-7}$$

$$R_A\mathrm{A} = K_A\frac{L_AW_{Cell}}{2\mu_{na}C_{GOX}V_{gs}} \tag{2-8}$$

$$R_{JFET}\mathrm{A} = \frac{\rho_D X_{JB}W_{Cell}}{2L_A} \tag{2-9}$$

$$R_{SUB}\mathrm{A} = \rho_{SUB} T_{SUB} \tag{2-10}$$

Here each structural parameter is shown in Fig. 2-3 and defined as follows. W_{Cell} is cell width, W_{G} is gate width, L_{CH} is channel length, L_{A} is accumulation layer length, X_{JB} is junction depth of p–base layer, $X_{\mathrm{JB\_l}}$ is lateral expansion width of the p–base layer, ρ_{D} is resistivity of n–drift layer, ρ_{SUB} is resistivity of n^+–substrate, and T_{SUB} is thickness of the n^+–substrate. In addition, μ_{ni} is electron mobility of inversion layer, μ_{na} is electron mobility of accumulation layer, C_{GOX} is gate oxide capacitance, V_{gs} is gate voltage, and V_{TH} is threshold voltage. K_{A} is a coefficient of considering current spreading from the accumulation region to the JFET region [25] [26]. K_{A} is assumed to be around 0.6.

Moreover, C_{gox}, ρ_{D} and ρ_{SUB} are expressed as

$$C_{GOX} = \frac{\varepsilon_{OX}\varepsilon_0}{T_{GOX}} \tag{2-11}$$

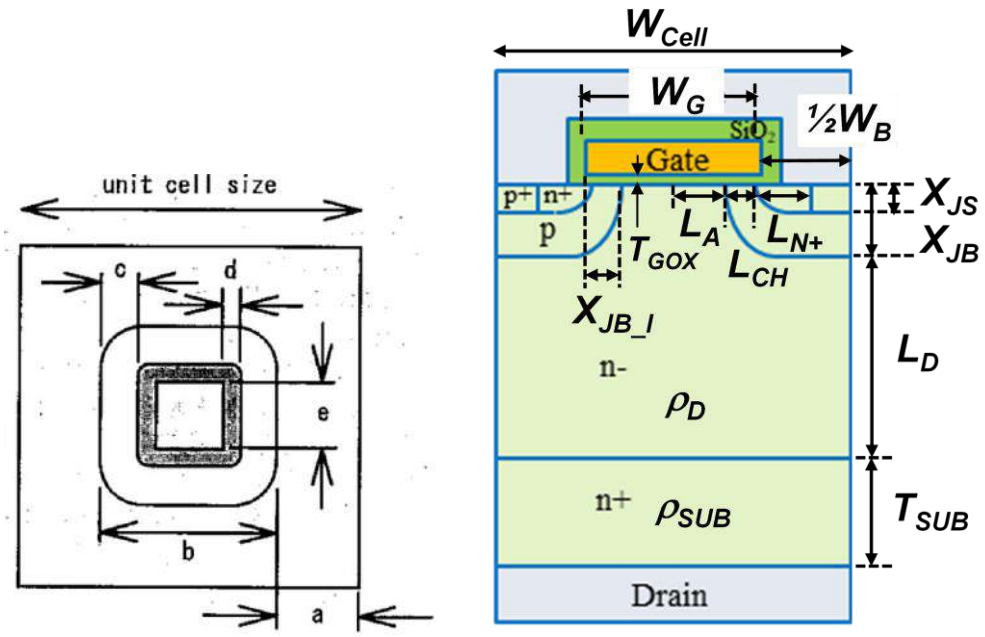
$$\rho_D = \frac{1}{q\mu_{n\_D}N_D} \tag{2-12}$$

$$\rho_{SUB} = \frac{1}{q\mu_{n\_SUB}N_{SUB}} \tag{2-13}$$

where $\varepsilon_{\mathrm{OX}}\varepsilon_0$ is the permittivity of silicon dioxide (SiO_2), T_{GOX} is the gate oxide thickness, and N_{SUB} is n^+–substrate concentration. In addition, q is elementally charge, $\mu_{\mathrm{n\_D}}$ is electron mobility of n–drift layer, and $\mu_{\mathrm{n\_SUB}}$ is electron mobility of n^+–substrate.

In the n–drift layer, current flow from the corner of the p–base layer spreads in angle of 45 degrees. $R_{\mathrm{D}}A$ model is divided into two cases, i.e., $W_{Cell} \geq 2(L_D + L_A)$ or $W_{Cell} < 2(L_D + L_A)$, and expressed as follows.

$$R_D\mathrm{A} = \begin{cases} \dfrac{\rho_D W_{Cell}}{2}\ln\dfrac{L_D + L_A}{L_A}, & W_{Cell} \geq 2(L_D + L_A) \\ \dfrac{\rho_D W_{Cell}}{2}\ln\dfrac{W_{Cell}}{2L_A} + \rho_D\left(L_D - \dfrac{W_B}{2} - X_{JB\_l}\right), & W_{Cell} < 2(L_D + L_A) \end{cases} \tag{2-14}$$



(a) (b

Fig. 2-3. (a) Top view of unit-cell layout [28] [29], © 1995 IEICE, and (b) structural parameters of D-MOSFET.

a: Half of gate poly-silicon width (1/2 W_G).

b: p–Base width (W_B).

c: Distance between gate poly-silicon and contact.

d: n^+–Source contact width.

e: p^+–Body contact width.

By the way, Eqs. (2-7)–(2-9) and (2-14) show the case of the stripe geometry of the D-MOSFET as a simplified. For example, in the $R_{CH}A$ (Eq. (2-7)), channel width per unit area A is given as $2W_{Cell}/{W_{Cell}}^2 = 2/W_{Cell}$ in stripe geometry. On the other hand, that is given as $4W_B/{W_{Cell}}^2$ in square cell geometry shown as Fig. 2-3(a). Each of the resistance included in Eq. (2-6) in the square cell geometry is expressed by amended model as below.

$$R_{CH}\mathrm{A} = \frac{L_{CH}{W_{Cell}}^2}{4W_B\mu_{ni}C_{GOX}(V_{gs} - V_{TH})} \tag{2-15}$$

$$R_A\mathrm{A} = K_A\frac{L_A{W_{Cell}}^2}{4(W_B + 2X_{JB\_l})\mu_{na}C_{GOX}V_{gs}} \tag{2-16}$$

$$R_{JFET}\mathrm{A} = \frac{\rho_D X_{JB} {W_{Cell}}^2}{{W_{Cell}}^2 - \left(W_B + 2X_{JB\_l}\right)^2} \tag{2-17}$$

$$R_D\mathrm{A} = R_{D1}A + R_{D2}A \tag{2-18}$$

$$R_{D2}\mathrm{A} = \begin{cases} 0 & , \quad W_{Cell} \geq 2(L_D + L_A) \\ \rho_D \left(L_D - \dfrac{W_{Cell}}{2} + L_A\right), & W_{Cell} < 2(L_D + L_A) \end{cases} \tag{2-19}$$

$$R_{D1}\mathrm{A} = \frac{R_{D1\_G}A \cdot R_{D1\_B}A}{R_{D1\_G}A + R_{D1\_B}A} \tag{2-20}$$

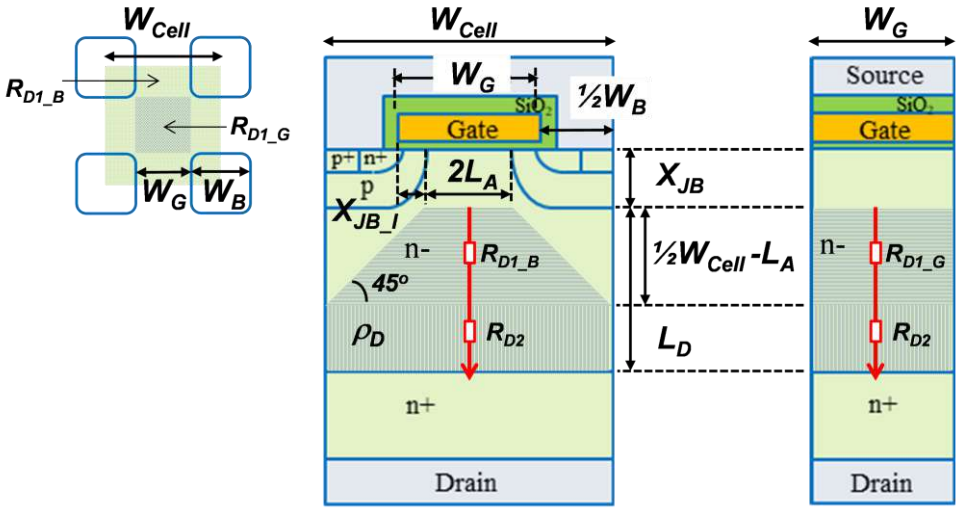
$$R_{D1\_G}\mathrm{A} = \frac{{W_{Cell}}^2}{{W_G}^2}\rho_D \left(\frac{W_{Cell}}{2} - L_A\right) \tag{2-21}$$

$$R_{D1\_B}\mathrm{A} = \begin{cases} \dfrac{\rho_D {W_{Cell}}^3}{2\left({W_{Cell}}^2 - {W_G}^2\right)} \ln \dfrac{L_D + L_A}{L_A}, & W_{Cell} \geq 2(L_D + L_A) \\ \dfrac{\rho_D {W_{Cell}}^3}{2\left({W_{Cell}}^2 - {W_G}^2\right)} \ln \dfrac{W_{Cell}}{2L_A}, & W_{Cell} < 2(L_D + L_A) \end{cases} \tag{2-22}$$

Here, $R_{D1}A$, $R_{D2}A$, $R_{D1\_G}A$ and $R_{D1\_B}A$ are components of the R_DA shown in Fig. 2-4. As expressed in Eq. (2-20), $R_{D1}A$ is expressed as a parallel resistance of $R_{D1\_G}A$ and $R_{D1\_B}A$. $R_{D1\_G}A$ in Eq. (2-21) expresses a component of the drift layer resistance under the gate intersection. In the same way, $R_{D1\_B}A$ in Eq. (2-22) expresses another component of the drift layer resistance, which is spreading from the end of the JFET region to under the p–base layer in angle of 45 degrees.

$R_{D1\_B}A$ and $R_{D2}A$ models are divided into two cases as same as the case of the stripe geometry, i.e., $W_{Cell} \geq 2(L_D + L_A)$ or $W_{Cell} < 2(L_D + L_A)$.

To improve the $R_{ON}{}^{DMOS}A$ with necessary V_B maintained, all the components of $R_{ON}{}^{DMOS}A$ have to be reduced by individual appropriate techniques.



(a) (b) (c)

Fig. 2-4. (a) Top view of D-MOSFET for square cell layout. Schematic cross-sectional structure, which shows components of the n–drift layer resistance (R_{D1_B}, R_{D1_G}, R_{D2}). (b) Current flow spreading in 45 degrees underneath p-base layer. (c) Current flow under gate intersection.

2.2.2. List of on-resistance model

Table 2-1. List of $R_{ON}A$ model equations for D-MOSFET (stripe and square cell design).

Stripe	Square cell
$R_{CH}\mathrm{A} = \dfrac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}$	$R_{CH}\mathrm{A} = \dfrac{L_{CH}{W_{Cell}}^2}{4W_B\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}$
$R_A\mathrm{A} = K_A\dfrac{L_AW_{Cell}}{2\mu_{na}C_{GOX}V_{gs}}$	$R_A\mathrm{A} = K_A\dfrac{L_A{W_{Cell}}^2}{4(W_B+2X_{JB\_l})\mu_{na}C_{GOX}V_{gs}}$
$R_{JFET}\mathrm{A} = \dfrac{\rho_DX_{JB}W_{Cell}}{2L_A}$	$R_{JFET}\mathrm{A} = \dfrac{\rho_DX_{JB}{W_{Cell}}^2}{{W_{Cell}}^2-(W_B+2X_{JB\_l})^2}$
$R_D\mathrm{A} = \dfrac{\rho_DW_{Cell}}{2}\ln\dfrac{W_{Cell}}{2L_A}+\rho_D\left(L_D-\dfrac{W_B}{2}-X_{JB_l}\right)$	$R_D\mathrm{A} = R_{D1}A + R_{D2}A$
$W_{Cell} < 2(L_D+L_A)$	$R_{D1}\mathrm{A} = \dfrac{R_{D1\_G}A\cdot R_{D1\_B}A}{R_{D1\_G}A+R_{D1\_B}A}$
	$R_{D1\_G}\mathrm{A} = \dfrac{{W_{Cell}}^2}{{W_G}^2}\rho_D\left(\dfrac{W_{Cell}}{2}-L_A\right)$
	$R_{D1\_B}\mathrm{A} = \dfrac{\rho_D{W_{Cell}}^3}{2({W_{Cell}}^2-{W_G}^2)}\ln\dfrac{W_{Cell}}{2L_A}$
	$R_{D2}\mathrm{A} = \rho_D\left(L_D-\dfrac{W_{Cell}}{2}+L_A\right)$
	$W_{Cell} < 2(L_D+L_A)$
$R_{SUB}\mathrm{A} = \rho_{SUB}T_{SUB}$	$R_{SUB}\mathrm{A} = \rho_{SUB}T_{SUB}$

2.2.3. On-resistance reduction techniques for 60-V D-MOSFET

In the $R_{ON}A$ of the D-MOSFET, there are main five components with comparatively high value; $R_{CH}A$, R_AA, $R_{JFET}A$, R_DA and $R_{SUB}A$, as shown in Eq. (2-6). Reduction of the whole $R_{ON}A$ is achieved by improving those components individually. In this subsection, two process techniques, which are unit-cell shrinking and shallow pn-junction formation, are applied to 60-V-class D-MOSFET and achieved results are described [28] [29].

2.2.3.1. Unit-cell shrinking by utilizing advanced design rule

It can consider from Eqs. (2-7) and (2-8) that both $R_{CH}A$ and R_AA are reduced by shrinking the unit-cell. By utilizing advanced design rule, e.g., 1.2-μm rule in mid-1990s, both W_G and W_B can be shrunk compared with those in conventional 2.5-μm rule. In the D-MOSFET cell layout shown in Fig. 2-3(a), each parameter is designed to an optimum dimension, e.g., (a) the W_G defined by the poly-silicon etching, (c) sufficient isolation distance between the gate poly-silicon and the contact, (d) n^+–source contact width keeping low-resistance, and (e) p^+–body contact width having stable V_B.

2.2.3.2. Shallow pn-junction formation by PSG sidewall process

The R_{JFET} region is made up of the p–base layer and the n–drift layer under the gate electrode. Therefore, it can consider from Eq. (2-9) that the $R_{JFET}A$ becomes smaller as the distance between the p–base layers ($2\times L_A$) becomes wider, or as the p–base layers depth (X_{JB}) becomes shallower.

The R_D region is under the JFET region and the p–base layers. The R_DA becomes smaller as the L_D becomes thinner. The necessary value of the L_D determined by the V_B in Eq. (2-2) has to consider the expansion of p–base layer diffusion and the extension of the high-density layer from the n^+–substrate after passing through the device fabrication process. Thus, the shallow p–base layer formation by adopting less annealing process is effective as a method to reduce the L_D.

Even when the X_{JB} is formed shallower, the L_{CH} has to keep a necessary length to prevent punch-through phenomenon, which leads to degrade the V_B. Therefore the X_{JS}, which is junction depth of the n^+–source layer, has to be moved away from the p–base layer edge in lateral direction at the same time. This can be achieved by using sidewall process and self-aligning n^+–diffusion layer, where PSG (phosphor-silicate glass) sidewalls are formed on both sides of the gate poly-silicon, as shown in Fig. 2-5.

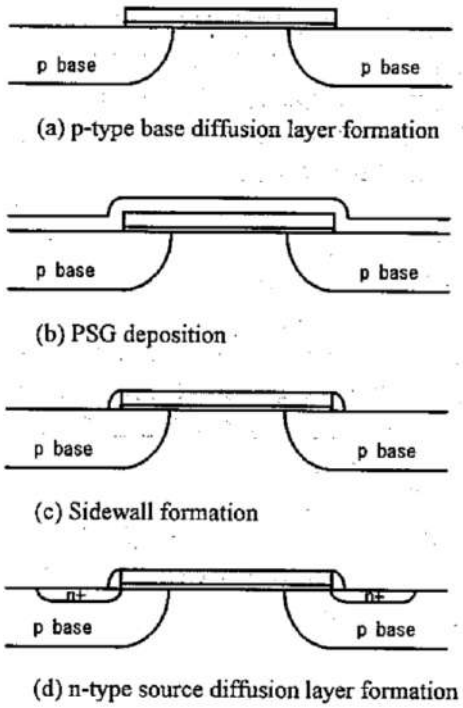


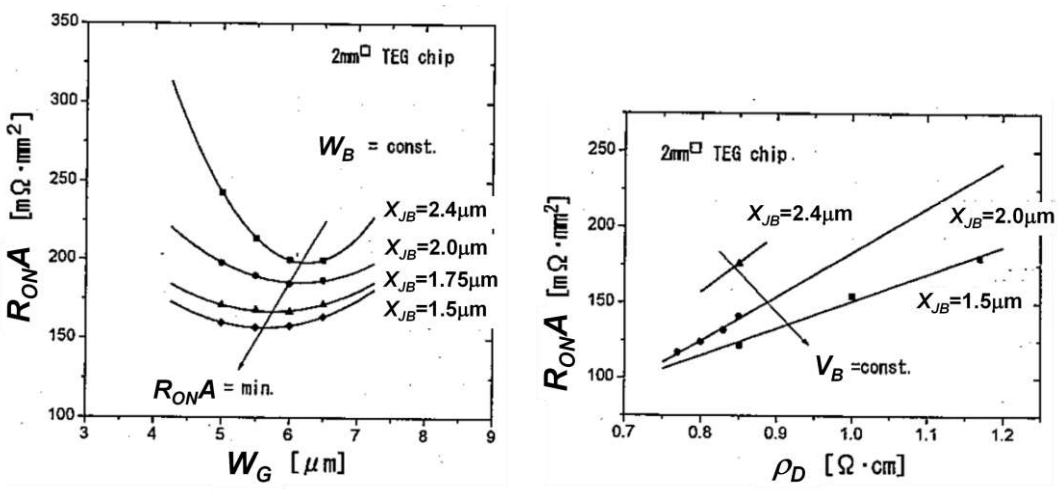
Fig. 2-5. Sidewall self-aligned process for n+ source layer formation. [29] © 1995 IEICE. (PSG: phosphor-silicate glass.)

2.2.3.1. Experimental results of $R_{ON}A$ reduction

In order to evaluate the $R_{ON}A$ reduction with newly developed process, a test element group (TEG), which plural 2×2 mm^2 chips were arranged, was fabricated. As evaluation of the TEG of D-MOSFET, both W_G and X_{JB} dependences of $R_{ON}A$, and both ρ_D and X_{JB} dependences of $R_{ON}A$ were shown in Fig. 2-6(a) and Fig. 2-6(b), respectively.

In a viewpoint of minimizing $R_{ON}A$, an optimum W_G became smaller with shallowing the X_{JB}. When the W_B was constant value of 6 μm and X_{JB} was 1.5 μm, the optimum W_G was approximately 5.5 μm. In the case that the W_G was narrower than the optimum value, the $R_{ON}A$ increased because the $R_{JFET}A$ component became large. However, the rate of $R_{ON}A$ increase were suppressed enough with respect to the shallower X_{JB}. It can mention that such a shallow pn-junction formation has advantage as a robust design regarding the W_G variation in the D-MOSFET cell.

In the case of lower ρ_D, not only the $R_{ON}A$ decreased but also the V_B decreased. Therefore, in order to satisfy both sufficient high V_B and smaller $R_{ON}A$, it was found that the V_B maintained by slightly high ρ_D with shallow X_{JB} was better choice than that by deeper X_{JB}.



(a) (b)

Fig. 2-6. (a) W_G and X_{JB} dependences of $R_{ON}A$, and (b) ρ_D and X_{JB} dependences of $R_{ON}A$ in fabricated TEG of D-MOSFET. [29] (modified).

Moreover, in this experiment, impurity doping of n^+–substrate was changed from phosphorus to arsenic to reduce the $R_{SUB}A$. As the effect, the ρ_{SUB} was reduced to one-thirds and it was less than 6 mΩ·cm.

As the experimental result shown in Fig. 2-7, $R_{ON}A$ of 130 mΩ·mm² with V_B of 70 V was achieved by adopting process techniques and optimization described in subsections 2.2.3.1–2.2.3.1.

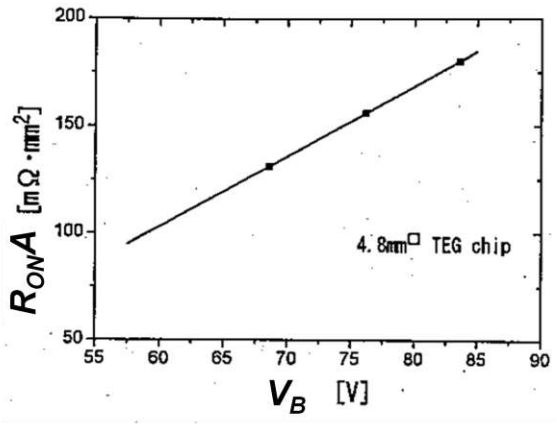


Fig. 2-7. Experimental result of relationship between $R_{ON}A$ and V_B in fabricated TEG of D-MOSFET. [29] (modified).

2.2.4. Validation of on-resistance model

Fig. 2-8 shows the $R_{ON}A$ of developed 60-V-class D-MOSFET compared with that of both analytical model and TCAD simulation. The structural parameters, electrical parameters and physical constants are indicated in Table 2-2, Table 2-3 and Table 2-4. For the stripe geometry, the $R_{ON}A$ calculated by the model corresponded to the TCAD result with only 2.4% error. For the square cell geometry, the $R_{ON}A$ calculated by the model corresponded to the experimental result with only 4.2% error.

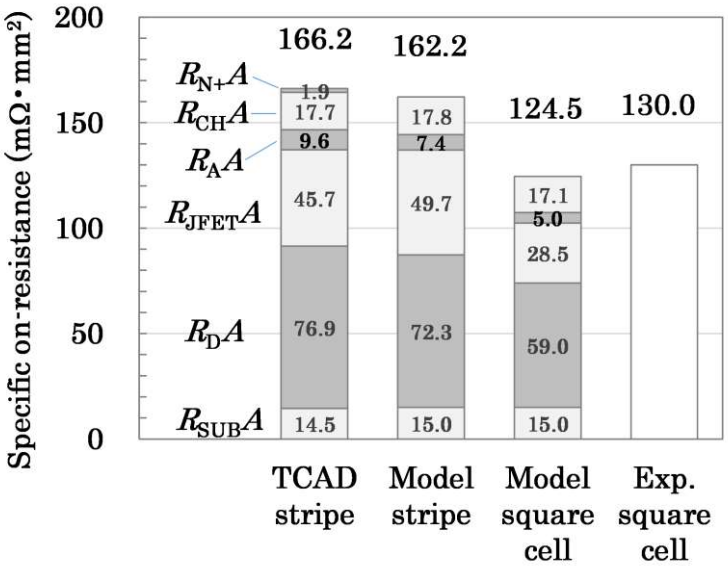


Fig. 2-8. Experimental result of $R_{ON}A$ for developed 60-V-class D-MOSFET compared with that of both analytical model and TCAD simulation.

Table 2-2. Structural parameters of 60-V-class D-MOSFET to calculate $R_{ON}A$.

Symbol	Parameters	Numerics	Unit
W_{Cell}	Cell width	11.5	μm
W_G	Gate width	5.50	μm
W_B	p–Base width	6.00	μm
L_{CH}	Channel length	1.00	μm
L_A	Accumulation length	1.48	μm
K_A	Coefficient of current spreading in the accumulation region	0.60	
T_{GOX}	Gate oxide thickness	0.05	μm
X_{JS}	n^+–Source junction depth	0.50	μm
X_{JB}	p–Base junction depth	1.50	μm
X_{JB_l}	p–Base junction lateral length	1.28	μm
L_D	n–Drift layer length	5.00	μm
ρ_D	Resistivity of n–drift layer	0.85	Ω・cm
N_D	Drift layer concentration	5.76×10^{15}	atoms/cm^3
T_{SUB}	n^+–Substrate thickness	250	μm
ρ_{SUB}	Resistivity of n^+–substrate	0.006	Ω・cm
N_{SUB}	n^+–Substrate concentration	9.70×10^{18}	atoms/cm^3

Table 2-3. Electrical parameters of 60-V-class D-MOSFET to calculate $R_{ON}A$.

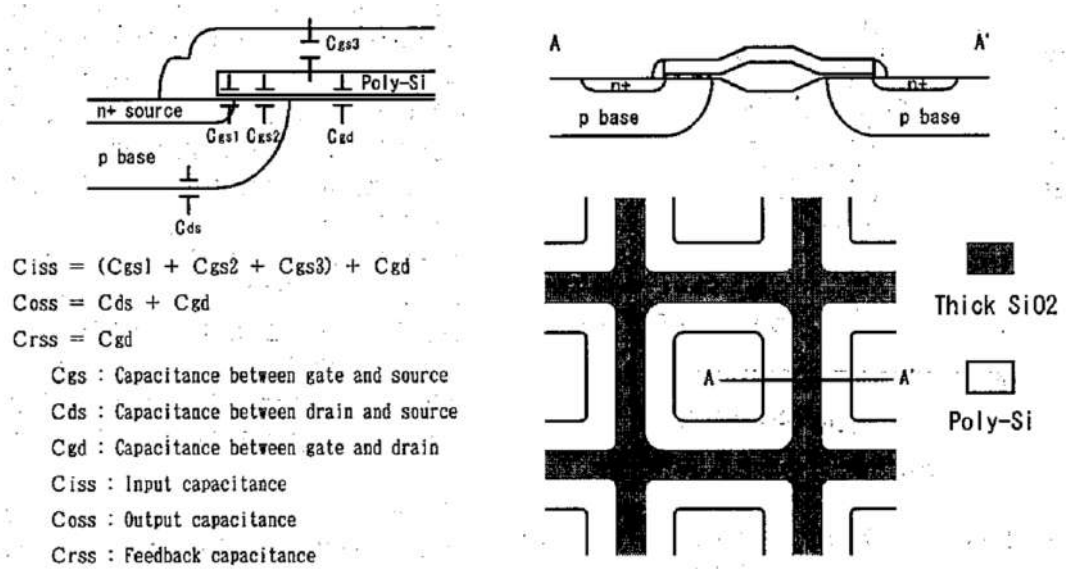
Symbol	Parameters	Numerics	Unit
V_{gs}	Gate–source voltage	10.0	V
V_{TH}	Threshold voltage	1.50	V
μ_{ni}	Electron mobility of inversion layer	550	cm^2/Vs
μ_{na}	Electron mobility of accumulation layer	1000	cm^2/Vs
μ_{n_D}	Electron mobility of n–drift layer	1250	cm^2/Vs
μ_{n_SUB}	Electron mobility of n^+–substrate	109	cm^2/Vs

Table 2-4. Physical constants to calculate $R_{ON}A$.

Symbol	Description	Property	Unit
q	Elementary charge	1.60×10^{-19}	C
ε_0	Permittivity in vacuum	8.854×10^{-14}	F/cm
ε_{Si}	Dielectric constant of Si	11.7	
ε_{OX}	Dielectric constant of SiO_2	3.9	

2.2.5. Improvement of parasitic capacitance by partially thick gate-oxide structure

Reduction of $R_{ON}A$ for D-MOSFET was achieved by unit-cell shrinking, shallow pn-junction formation, and high impurity doping of n^+–substrate. On the other hand, parasitic capacitances of the D-MOSFET are improved by other design approach. Fig. 2-9(a) shows the parasitic capacitances of the D-MOSFET: input capacitance (C_{iss}), output capacitance (C_{oss}), and reverse transfer capacitance (feedback capacitance) (C_{rss}). Among those, gate–drain capacitance C_{gd} can be reduced by partially thick gate-oxide structure as shown in Fig. 2-9(b).



(a) (b)

Fig. 2-9. (a) Parasitic capacitances of D-MOSFET. (b) Partially thick .gate oxide structure for D-MOSFET. [29] © 1995 IEICE.

C_{rss} equals to C_{gd}, and both C_{iss} and C_{oss} include C_{gd}. Therefore, in the experimental results, all parasitic capacitances were reduced by the partially thick gate-oxide structure, as shown in Fig. 2-10.

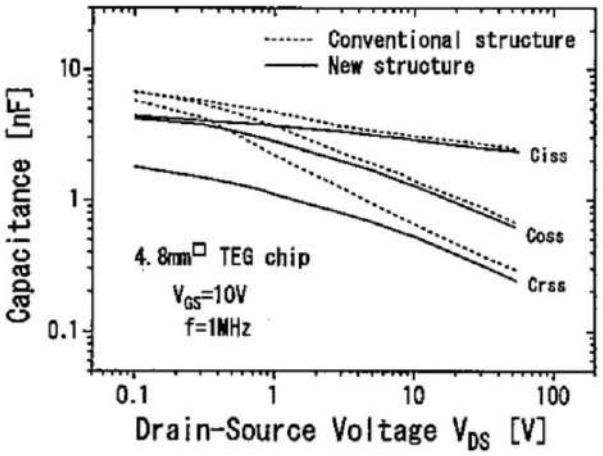


Fig. 2-10. V_{ds} dependence of capacitances (C_{iss}, C_{oss}, and C_{rss}) in D-MOSFETs. In comparison of conventional structure and fabricated partially thick gate oxide structure. [29] © 1995 IEICE.

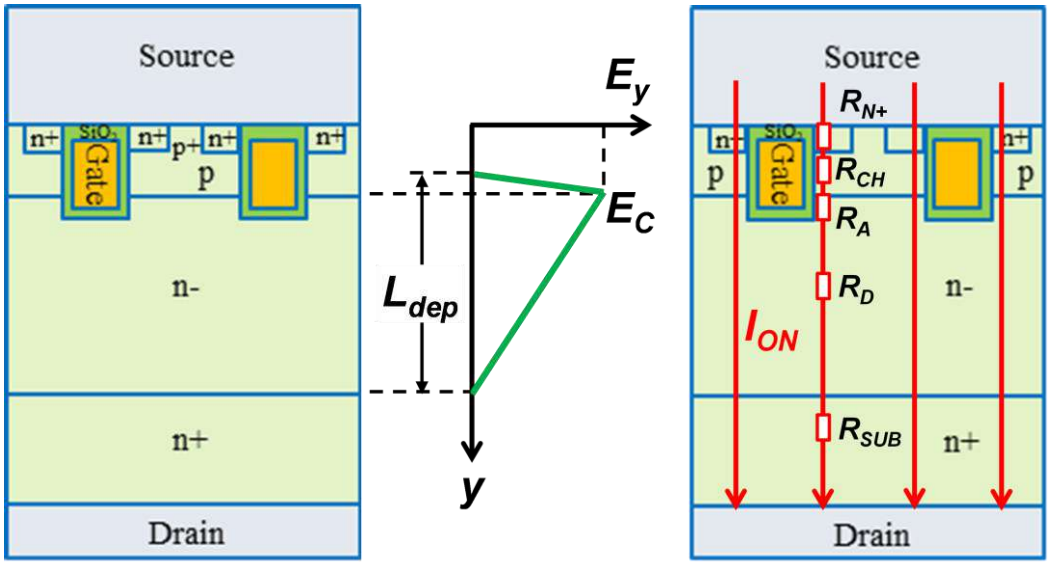
2.3. High-density trench gate MOSFET (U-MOSFET)

2.3.1. Basic structure and on-resistance ($R_{ON}A$) components of U-MOSFET

Schematic cross-sectional structure of U-MOSFET for two unit-cells area is shown in Fig. 2-11. Fig. 2-11(a) shows a distribution of electric field E_y of drift layer in vertical direction y, when reverse bias applies to drain. In the U-MOSFET, V_B of one-dimensional plane pn-junction is determined by the area of this triangle electric field in a similar manner to the D-MOSFET. When a trench gate penetration from a p–base layer is relatively short, the V_B of the U-MOSFET is approximated as same Eqs. (2-2)–(2-4).

Fig. 2-11(b) shows on-state current paths and on-resistance components of the U-MOSFET. The $R_{N+}A$ is more negligible than that of the D-MOSFET, and the $R_{ON}A$ of the U-MOSFET ($R_{ON}{}^{UMOS}A$) can be approximated by using main components,

$$R_{ON}{}^{UMOS}\mathrm{A} \approx R_{CH}A + R_A A + R_D A + R_{SUB}A. \tag{2-23}$$



(a) (b)

Fig. 2-11. Schematic cross-sectional structure of U-MOSFET, which shows two unit-cells area. (a) Electric field distribution in vertical direction of off-state. (b) On-state current paths and components of on-resistance.

In Eq. (2-23), $R_{CH}A$, R_AA and R_DA are divided into two cases, i.e., the U-MOSFET design is stripe geometry or square cell geometry. Fig. 2-12(a) shows structural parameters of the U-MOSFET. As shown in Fig. 2-12(b) and Fig. 2-12(c), channel width per unit area "A" is shown as $2W_{Cell}/{W_{Cell}}^2 = 2/W_{Cell}$ in stripe cell design, or $4W_{Mesa}/{W_{Cell}}^2$ in square cell design. Here, W_{Cell} is cell width and W_{Mesa} is mesa width.

$R_{CH}A$, R_AA and $R_{SUB}A$ in Eq. (2-23) are expressed by analytical model as below.

$$R_{CH}\mathrm{A} = \begin{cases} \dfrac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}\left(V_{gs}-V_{TH}\right)}, & \text{in stripe cell} \\ \dfrac{L_{CH}{W_{Cell}}^2}{4W_{Mesa}\mu_{ni}C_{GOX}\left(V_{gs}-V_{TH}\right)}, & \text{in square cell} \end{cases} \tag{2-24}$$

$$R_A\mathrm{A} = \begin{cases} K_A\dfrac{(2L_A+W_T)W_{Cell}}{4\mu_{na}C_{GOX}V_{gs}}, & \text{in stripe cell} \\ K_A\dfrac{(2L_A+W_T){W_{Cell}}^2}{8W_{Mesa}\mu_{na}C_{GOX}V_{gs}}, & \text{in square cell} \end{cases} \tag{2-25}$$

$$R_{SUB}\mathrm{A} = \rho_{SUB}T_{SUB} \tag{2-26}$$

Here, W_T is trench width and other same symbols are the same as those of subsection 2.2.1, i.e., L_{CH} is channel length, L_A is accumulation length, ρ_D is resistivity of n–drift layer, ρ_{SUB} is resistivity of n^+–substrate, T_{SUB} is thickness of the n^+–substrate, μ_{ni} is electron mobility of inversion layer, μ_{na} is electron mobility of accumulation layer, C_{GOX} is gate oxide capacitance, V_{gs} is gate voltage, and V_{TH} is threshold voltage. K_A is a coefficient of considering current spreading from the accumulation region to the drift region [25] [26]. In Eq. (2-25), the total accumulation length of the unit cell is given by $2L_A + W_T$. K_A is assumed to be around 0.6.

In addition, R_DA in Eq. (2-23) is consists of sub-components which are $R_{D1}A$, $R_{D2}A$, $R_{D1\_T}A$ and $R_{D1\_M}A$ as shown in Fig. 2-13, and is expressed by analytical model as below.

$$R_D\mathrm{A} = R_{D1}A + R_{D2}A \tag{2-27}$$

$$R_{D1}\mathrm{A} = \begin{cases} \dfrac{\rho_D W_{Cell}}{2}\ln\dfrac{W_{Cell}}{W_T}, & \text{in stripe cell} \\ \dfrac{R_{D1\_T}A\cdot R_{D1\_M}A}{R_{D1\_T}A+R_{D1\_M}A}, & \text{in square cell} \end{cases} \tag{2-28}$$

$$R_{D2}\mathrm{A} = \rho_D \left(L_D - L_A - \frac{W_{Mesa}}{2} \right) \tag{2-29}$$

$$R_{D1\_T}\mathrm{A} = \frac{{W_{Cell}}^2}{{W_T}^2} \rho_D \frac{W_{Mesa}}{2} \tag{2-30}$$

$$R_{D1\_M}\mathrm{A} = \frac{\rho_D {W_{Cell}}^3}{2\left({W_{Cell}}^2 - {W_T}^2\right)} \ln \frac{W_{Cell}}{W_T} \tag{2-31}$$

As expressed in Eq. (2-28), $R_{D1}A$ is a drift layer resistance spreading from under the trench to center of the mesa. Moreover, in the square cell, $R_{D1}A$ is expressed as a parallel resistance of $R_{D1\_T}A$ and $R_{D1\_M}A$. $R_{D1\_T}A$ in Eq. (2-30) expresses a component of the drift layer resistance under the trench intersection. In the same way, $R_{D1\_M}A$ in Eq. (2-31) expresses another component of the drift layer resistance, which is spreading from four sides surrounding the square mesa region.

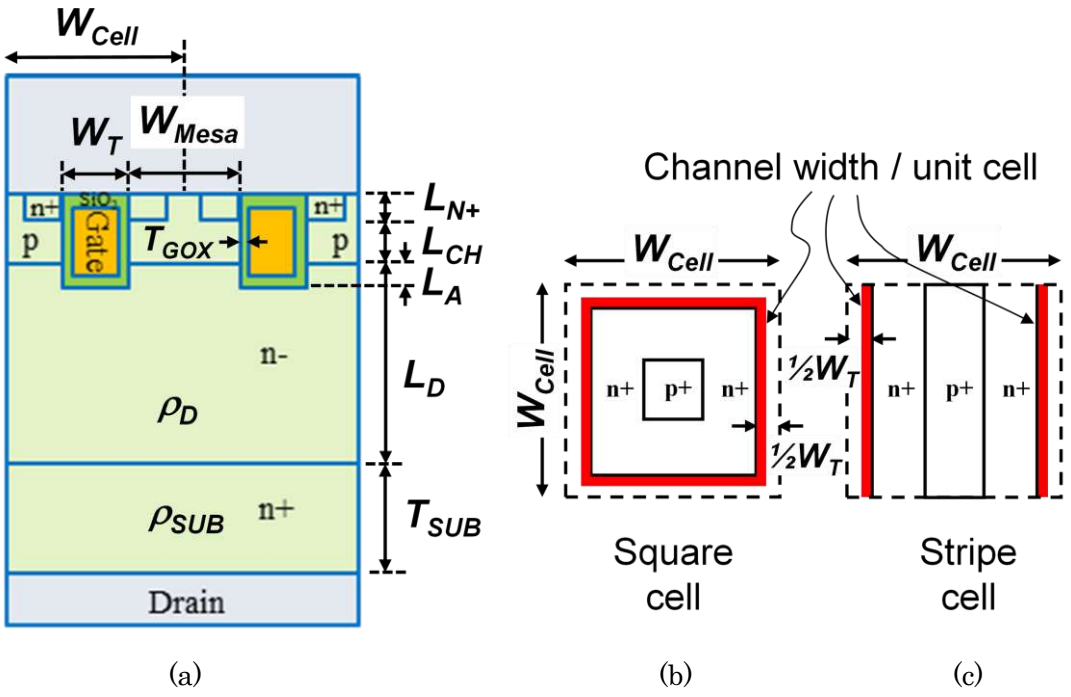
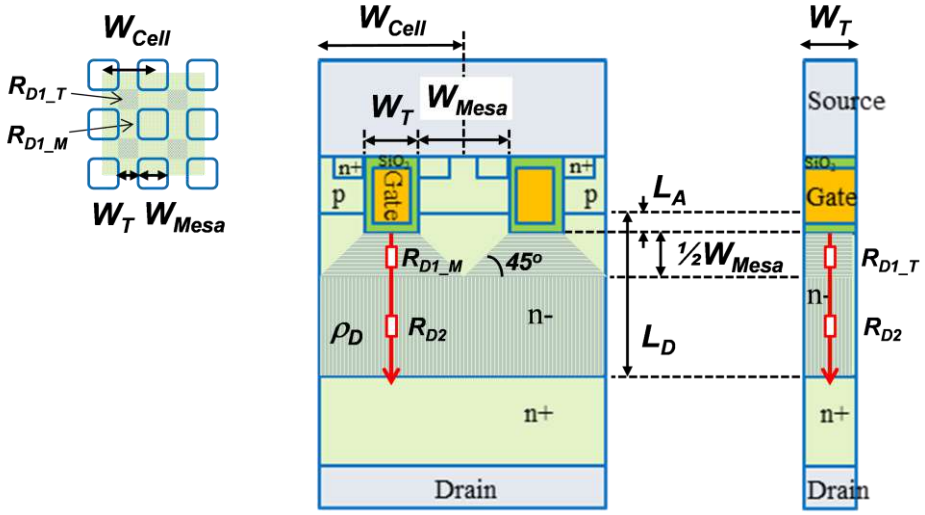


Fig. 2-12. (a) Structural parameters of U-MOSFET. Top view of U-MOSFET unit-cell layout for (b) square cell design and (c) stripe cell design.

To improve the $R_{ON}{}^{UMOS}A$ with necessary V_B maintained, all the components of $R_{ON}{}^{UMOS}A$ have to be reduced by individual appropriate techniques.

In the case of n^+/p^+ interactive layout pattern, $R_{CH}A$ is expressed as below.

$$R_{CH}\mathrm{A} = \frac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}(V_{gs}-V_{TH})} \cdot \frac{1}{Ratio_{np}} \tag{2-32}$$



(a) (b) (c)

Fig. 2-13. (a) Top view of U-MOSFET for square cell layout. Schematic cross-sectional structure, which shows components of the n–drift layer resistance (R_{D1_M}, R_{D1_T}, R_{D2}). (b) Current flow spreading in 45 degrees from four sides surrounding the square mesa region. (c) Current flow under trench intersection.

2.3.2. List of on-resistance model

Table 2-5. List of $R_{ON}A$ model equations for U-MOSFET (stripe and square cell design).

Stripe	Square cell
$R_{CH}\mathrm{A} = \dfrac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}$	$R_{CH}\mathrm{A} = \dfrac{L_{CH}{W_{Cell}}^2}{4W_{Mesa}\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}$
$\left[R_{CH}\mathrm{A} = \dfrac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}\cdot\dfrac{1}{Ratio_{np}}\right]$	
$R_A\mathrm{A} = K_A\dfrac{(2L_A+W_T)W_{Cell}}{4\mu_{na}C_{GOX}V_{gs}}$	$R_A\mathrm{A} = K_A\dfrac{(2L_A+W_T){W_{Cell}}^2}{8W_{Mesa}\mu_{na}C_{GOX}V_{gs}}$
$R_D\mathrm{A} = R_{D1}A + R_{D2}A$	$R_D\mathrm{A} = R_{D1}A + R_{D2}A$
$R_{D1}\mathrm{A} = \dfrac{\rho_D W_{Cell}}{2}\ln\dfrac{W_{Cell}}{W_T}$	$R_{D1}\mathrm{A} = \dfrac{R_{D1\_T}A\cdot R_{D1\_M}A}{R_{D1\_T}A + R_{D1\_M}A}$
$R_{D2}\mathrm{A} = \rho_D\left(L_D - L_A - \dfrac{W_{Mesa}}{2}\right)$	$R_{D1\_T}\mathrm{A} = \dfrac{{W_{Cell}}^2}{{W_T}^2}\rho_D\dfrac{W_{Mesa}}{2}$
	$R_{D1\_M}\mathrm{A} = \dfrac{\rho_D{W_{Cell}}^3}{2({W_{Cell}}^2-{W_T}^2)}\ln\dfrac{W_{Cell}}{W_T}$
	$R_{D2}\mathrm{A} = \rho_D\left(L_D - L_A - \dfrac{W_{Mesa}}{2}\right)$
$R_{SUB}\mathrm{A} = \rho_{SUB}T_{SUB}$	$R_{SUB}\mathrm{A} = \rho_{SUB}T_{SUB}$

2.3.3. Cell pitch shrinking by double trenches structure

Fig. 2-14 shows a U-MOSFET structure designed to square cell. In this design, the W_{Cell} can be drastically shrunk by adopting double trenches process, which means formation of trench gate and trench contact. The trench contact structures with metal plug have been reported [7] [30] [31] and 1.6–2.0 μm cell pitches have already been realized [32] [33]. In the U-MOSFET, the W_G in the case of the D-MOSFET is reduced to a W_T due to vertical trench gate electrode, and the W_B in the case of the D-MOSFET is also reduced to a W_{Mesa} due to adopting narrow trench contact opening width.

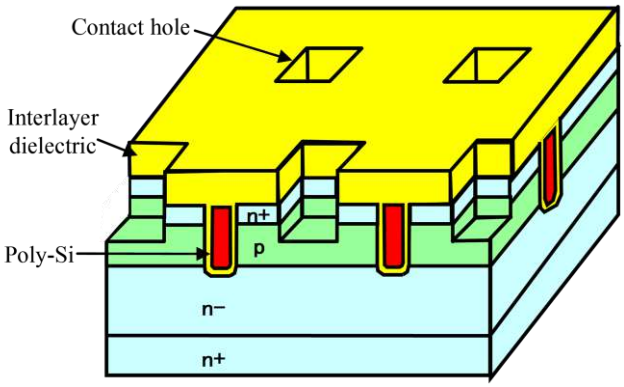


Fig. 2-14. Bird's eye view of U-MOSFET structure designed to square cell, which has double trenches in unit cell. (Source and drain metals are not shown.) [40] © 2007 IEEE, [41]

The representative process flow of the U-MOSFET having double trenches is disclosed in [34], and shown in Fig. 2-15(a)–(k).

(a) An n^-–epitaxial layer on n^+–substrate.
(b) Deposition of insulating layers consisted of silicon dioxide and silicon nitride, followed by trench forming by photo-lithography and reactive ion-etching (RIE).
(c) Rounding treatment of the trench corners by sacrificial oxidation or chemical dry etching (CDE).
(d) Gate poly-silicon deposition by low-pressure chemical vapor deposition (LP-CVD).
(e) Gate poly-silicon filling down to appropriate depth inside trench by RIE. Then, p–base and n^+–source formation by ion-implantation, followed by thermal annealing.
(f) Inter-layer insulating film deposition by LP-CVD, followed by thermal annealing.
(g) Trench contact forming by photo-lithography and RIE down to appropriate depth *d*.
(h) p^+–Body layer formation by ion-implantation and thermal annealing. Then barrier metal (like titanium nitride) sputtering.

(i) Forming contact plug material (like tungsten) by CVD.

(j) Etching-back the contact plug material.

(k) Thick metal (like aluminum) formation on the device surface, followed by source/gate electrodes patterning by photo-lithography and RIE. Then grinding and polishing back-surface, followed by back-surface metal formation for drain electrode.

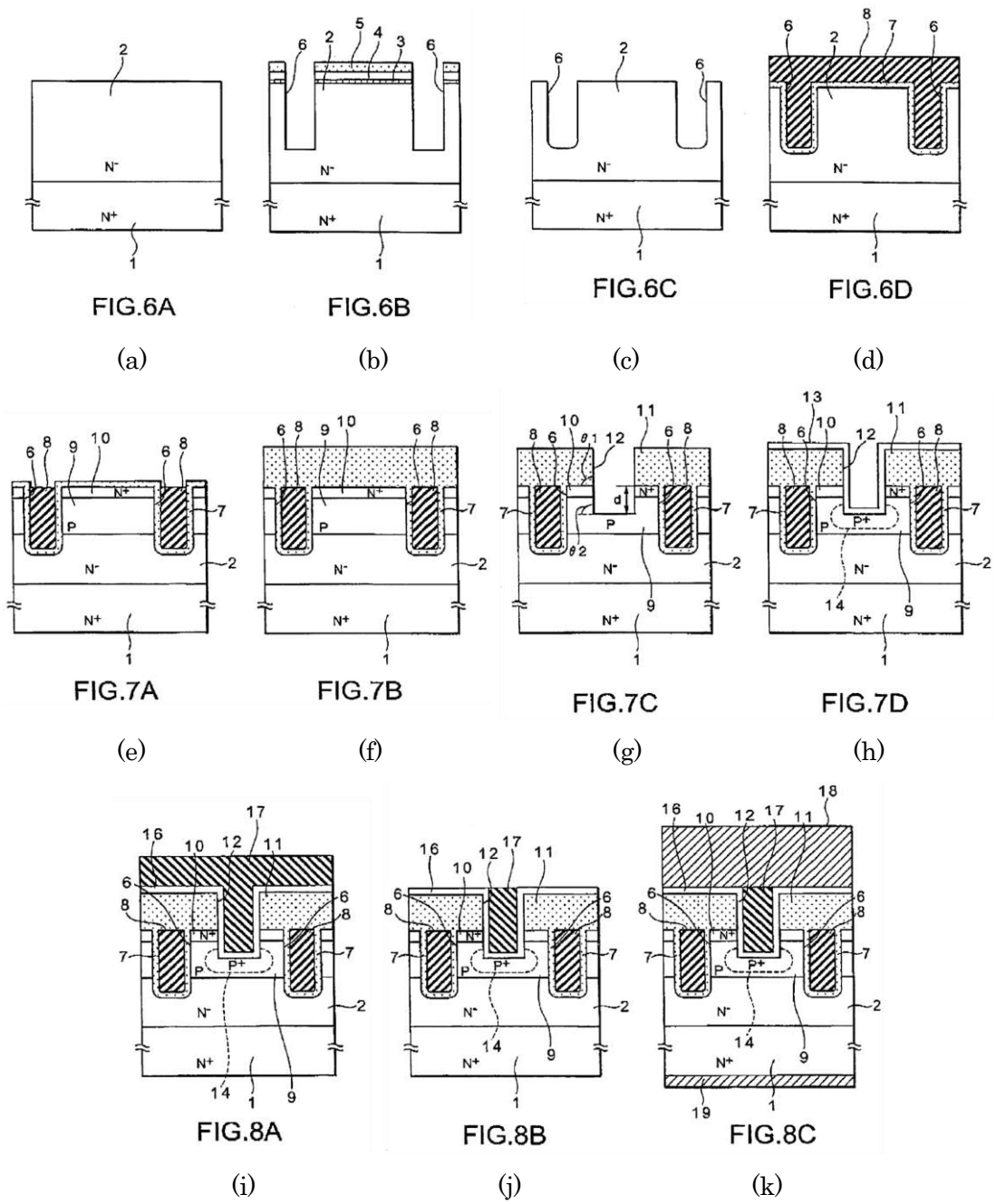


Fig. 2-15. Process flow of U-MOSFET having double trenches [34].

2.3.4. 30-V sub-micron cell pitch U-MOSFET applying by burying interlayer dielectric inside trench [1]

For the low-voltage U-MOSFETs, various unit cell structures have been proposed to shrink the cell size and to achieve high performance. Self-aligned contact structures realized by burying interlayer dielectric above poly-silicon gate inside trench was presented in [35] [36] [37]. High density trench structures around 1.0-μm-pitch were realized in p-channel U-MOSFET firstly [38] and accumulation-mode n-channel U-MOSFET also [39].

In this subsection, a newly developed sub-micron cell pitch 30-V-class n-channel U-MOSFETs are described [40] [41]. In the narrow pitch U-MOSFET structure, a plural layered oxide as interlayer dielectric (ILD) inside trench and the self-aligned contact are adopted. This structure accomplishes the unit cell pitch less than 1.0 μm. In addition, structural parameters are optimized to achieve the lowest on-resistance performance for both new rectangular cell design and stripe cell design.

2.3.4.1. Unit-cell design for total channel width maximization

As described in subsection 2.3.2, in the square cell design, although the unit cell size is defined by W_T and W_{Mesa}, the W_{Mesa} consists of three critical dimensions which are the trench contact width and the n^+–source width in both sides of the trench contact.

Fig. 2-16(a) shows the fabricated n-channel U-MOSFET structure of rectangular cell design, where n^+–source regions are divided by a p^+–body region in a cell. In addition, Fig. 2-16(b) shows the stripe cell design with alternatively arranged n^+/p^+ pattern in longer direction of trench. In both structures, since the ILD is completely buried inside trench, the surface of mesa region, which consists of n^+–source and p^+–body, can contact directly to source metal (not shown in the figures). Thus the self-aligned contact structure is realized in these cell design. Moreover, the unit cell size is given by sum of just two parameters, i.e., W_T and W_{Mesa} which equals to the contact width.

In the rectangular cell design, adjacent cells are arranged each other with a half pitch shift of the cell in longer direction. In this design, cross points of the orthogonal trenches, which form depressions above the gate poly-silicon, are avoided.

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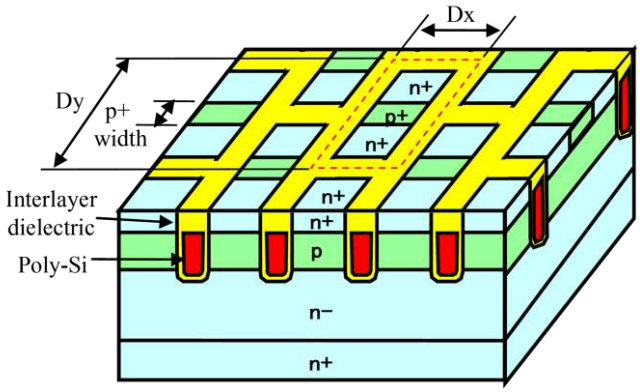
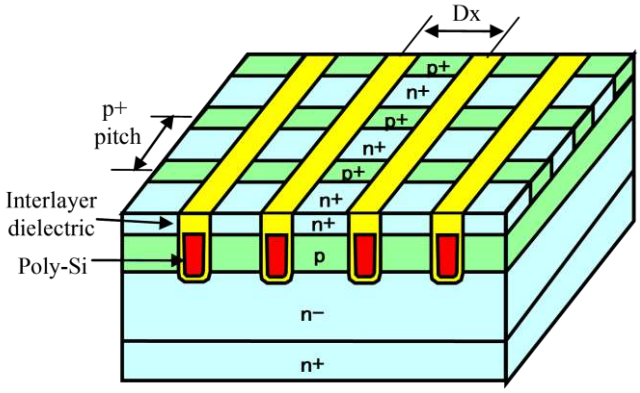
[1] Subsection 2.3.4 is reproduction of [40] chapter II and III, © 2007 IEEE, and a part of description is modified and comprehensive explanations are additionally provided.



(a) Rectangular cell design.



(b) Stripe cell design.

Fig. 2-16. Bird's eye view of newly developed U-MOSFETs structures. (Source and drain metals are not shown.) D_x is trench pitch in narrower direction for both rectangular cell and stripe cell. D_y is unit-cell length for rectangular cell. [40] © 2007 IEEE, [41]

Fig. 2-17(a) shows the U-MOSFET unit-cell layout of 2.0-μm-pitch square cell design, which structure corresponds to Fig. 2-14. The channel width of the unit square cell is sum of four sides surrounding trenches. Fig. 2-17(b) shows sub-micron-pitch rectangular cell design, which structure corresponds to Fig. 2-16(a). The channel width of the unit rectangular cell is double of sum of three sides surrounding trenches. Fig. 2-17(c) shows sub-micron-pitch stripe cell design, which structure corresponds to Fig. 2-16(b). The channel width of the unit stripe cell is double of sum of two sides along trenches.

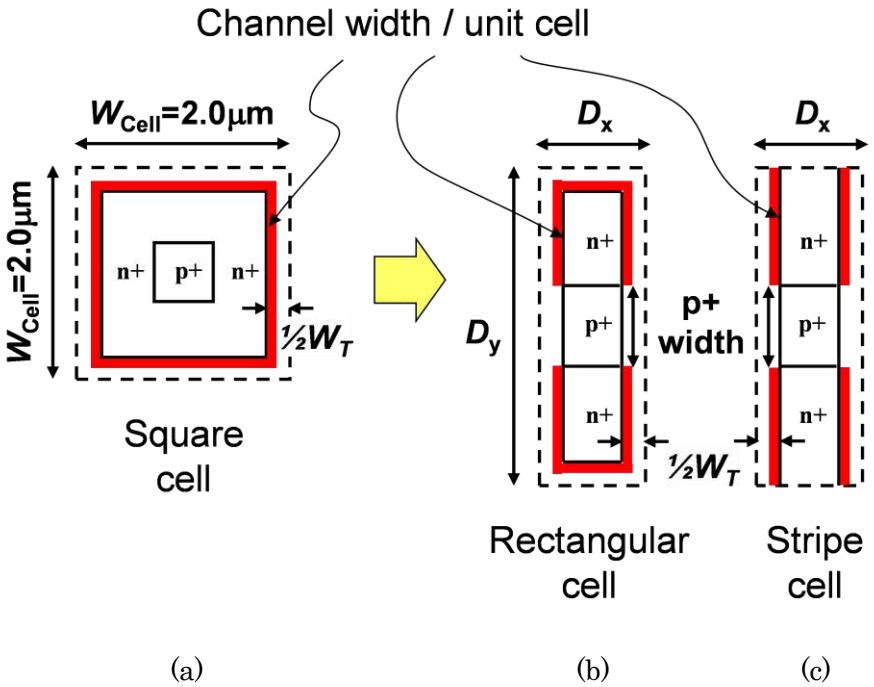
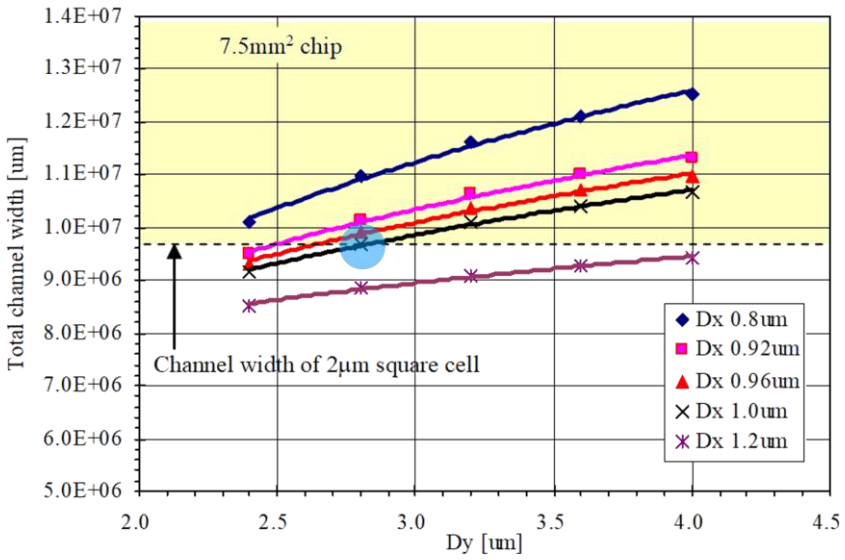


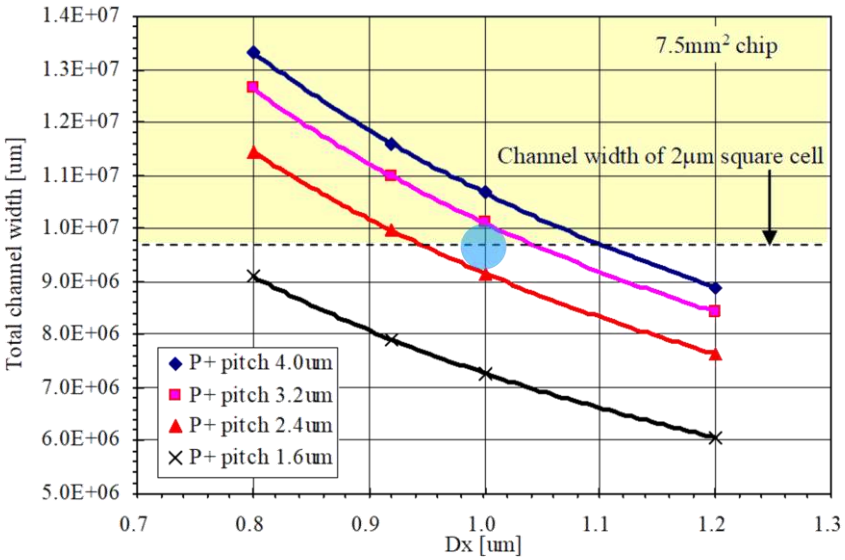
Fig. 2-17. Top views of U-MOSFET unit-cell layout for (a) 2-μm-pitch square cell design, (b) sub-micron-pitch rectangular cell design, and (c) sub-micron-pitch stripe cell design.

Fig. 2-18(a) and Fig. 2-18(b) show calculated total channel width in 7.5 mm^2 chip area for the rectangular cell design and the stripe cell design, respectively. In the rectangular cell, the total channel width increases with longer unit-cell length D_y in all investigated trench pitch D_x (0.8–1.2 μm). In the stripe cell, the total channel width becomes larger with respect to narrower trench pitch D_x.

The total channel width of the above two structures are compared with that of 2.0-μm square cell for the same chip area. The channel density of the rectangular cell exceeds that of the square cell at D_y > 2.8 μm (D_x = 1.0 μm), and thus, the channel resistance can be reduced. For the stripe design, almost the same effect is obtained at D_x < 1.0 μm (D_y = 2.8 μm). In both cases, p^+–pitch (D_y) and p^+–width are designed to maintain the avalanche robustness.



(a) Rectangular cell design



(b) Stripe cell design

Fig. 2-18. Calculated total channel width in 7.5 mm² chip area for (a) rectangular cell design, which depends on D_y, and (b) stripe cell design, which depends on D_x and p^+–pitch. Channel width of 2-μm square cell is indicated in both graphs for comparison. [40] © 2007 IEEE (modified), [41].

Fig. 2-19(a)–(c) show the simulated potential contours for narrow pitch U-MOSFETs for D_x = 0.8 μm, 1.0 μm, and 1.2 μm, respectively. In each simulation, the electrical potential under the trench bottom level was uniformly distributed, and the V_B was over 30 V. In the narrow pitch rectangular cell (or the stripe cell), the narrow space between trenches causes uniform potential distribution and the resulting V_B is higher than that of the square cell. In the present structure, the epi-thickness can be reduced by 0.2 μm and the epi-resistance component of the U-MOSFET can also be reduced.

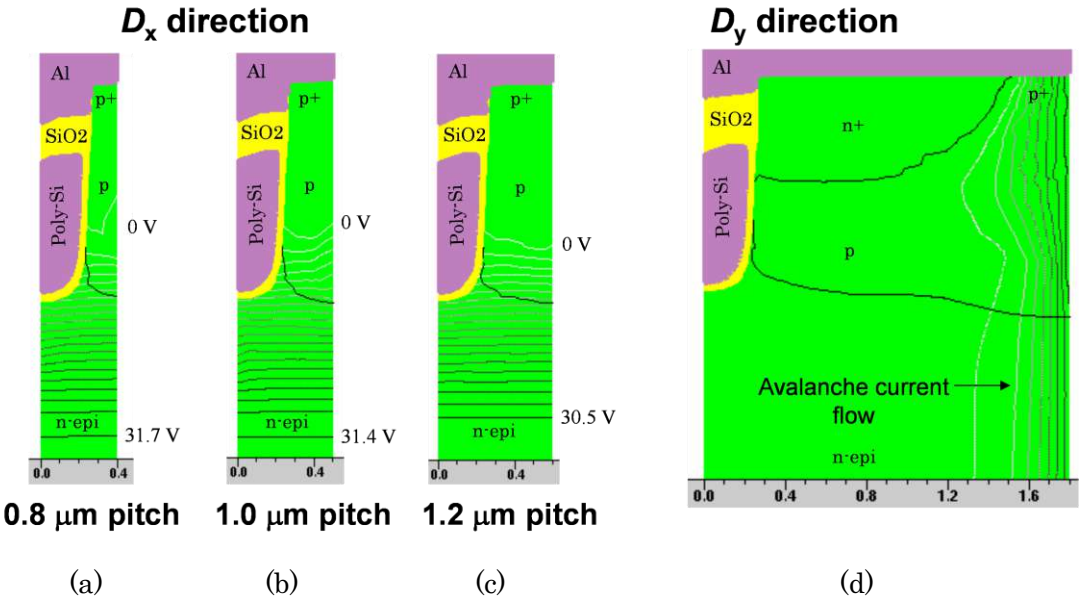


Fig. 2-19. Simulated potential contours for U-MOSFETs. In short side (D_x) direction, half size of (a) 0.8-μm pitch, (b) 1.0-μm pitch and (c) 1.2-μm pitch, which correspond to both stripe and rectangular cell, are simulated at p^+–region. In long side (D_y) direction, (d) half size of rectangular cell is simulated. [40] (c) 2007 IEEE (modified), [41] (modified).

2.3.4.2. Process flow and essential process evaluation

The representative process flow of narrow pitch rectangular cell U-MOSFET is disclosed in [42], and shown in Fig. 2-20(a)–(g) and Fig. 2-21(h)–(i).

(a) An n^-–epitaxial layer on n^+–substrate.

(b) Deposition of insulating layers consisted of silicon dioxide and silicon nitride, followed by trench forming by photo-lithography and reactive ion-etching (RIE).

(c) Rounding treatment of the trench corners by sacrificial oxidation or chemical dry etching (CDE).

(d) Gate oxidation and gate poly-silicon deposition by low-pressure chemical vapor deposition (LP-CVD).

(e) Gate poly-silicon filling down to appropriate depth inside trench by RIE.

(f) Inter-layer insulating film deposition by LP-CVD, followed by planarization by thermal annealing and etching-back to silicon surface by RIE.

(g) p–Base formation by ion-implantation, followed by thermal annealing. Then n^+–source formation by photo-lithography and ion-implantation.

(h) p^+–Body formation by photo-lithography and ion-implantation, followed by thermal annealing.

(i) Barrier metal (like titanium nitride) and thick metal (like aluminum) sputtering on the device surface, followed by source / gate electrodes patterning by photo-lithography and RIE.

Then grinding and polishing back-surface, followed by back-surface metal formation for drain electrode.

The main points of the sub-micron cell pitch U-MOSFET are described below. The trenches are formed by 0.25-μm design rule process and have 1.0-μm deep. The interlayer dielectric between the gate poly-silicon and the source metal is fabricated by two types of oxide. Firstly, Tetraethyl Orthosilicate (TEOS) is formed for good step coverage. Then, Boron-Phosphor Silicate Glass (BPSG) is deposited, which has good reflow properties in following thermal annealing.

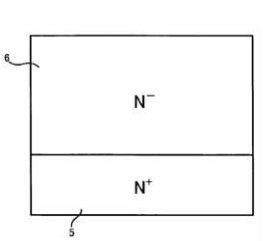


Fig. 5

(a)

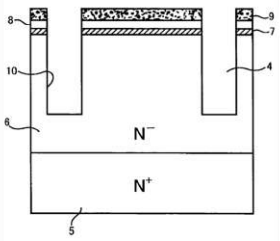


Fig. 6

(b)

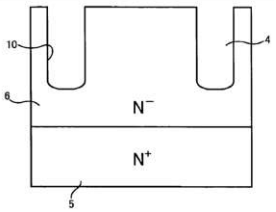


Fig. 7

(c)

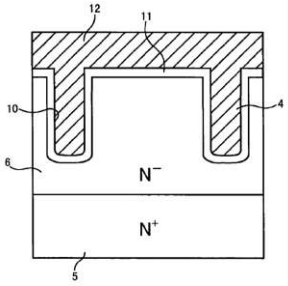


Fig. 8

(d)

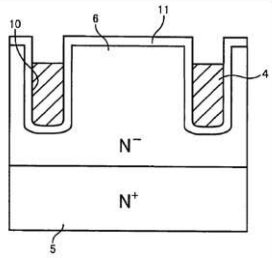


Fig. 9

(e)

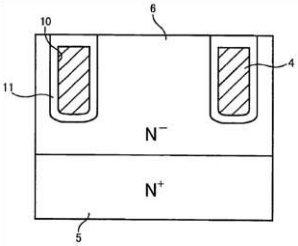


Fig. 10

(f)

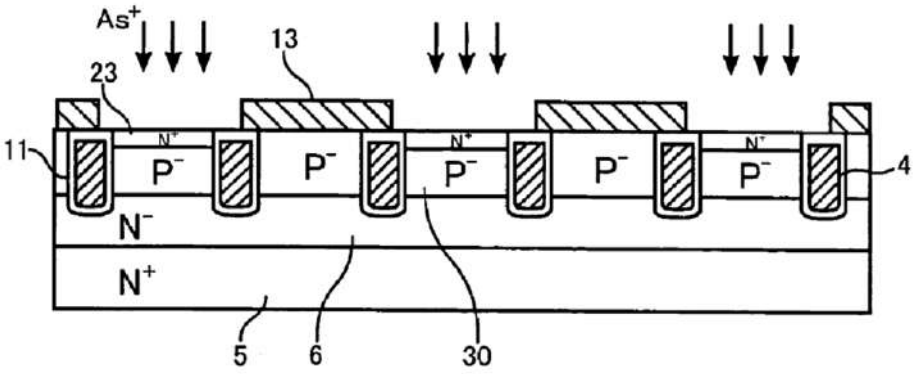


Fig. 11A

(g)

Fig. 2-20. Process flow of narrow pitch rectangular cell U-MOSFET. [42]

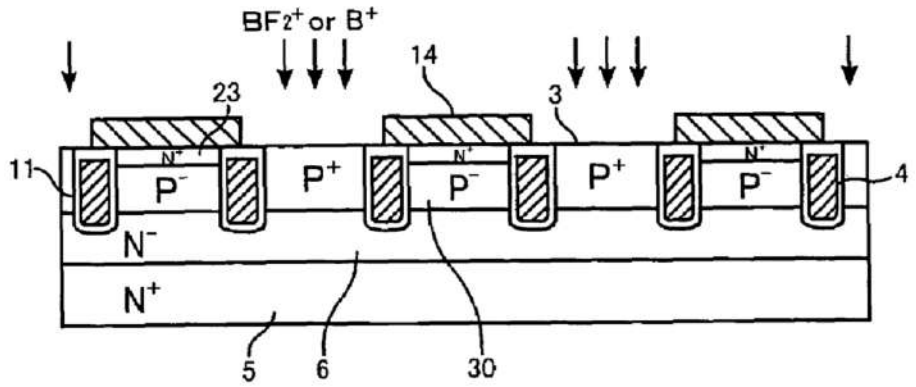


Fig. 13A

(h)

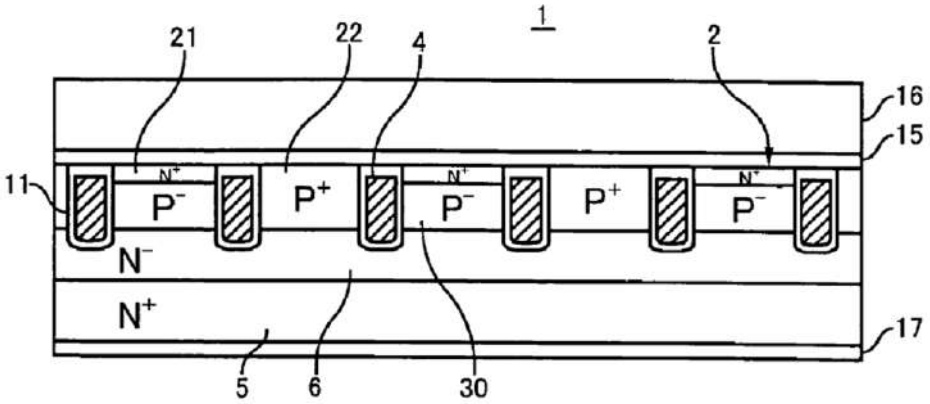
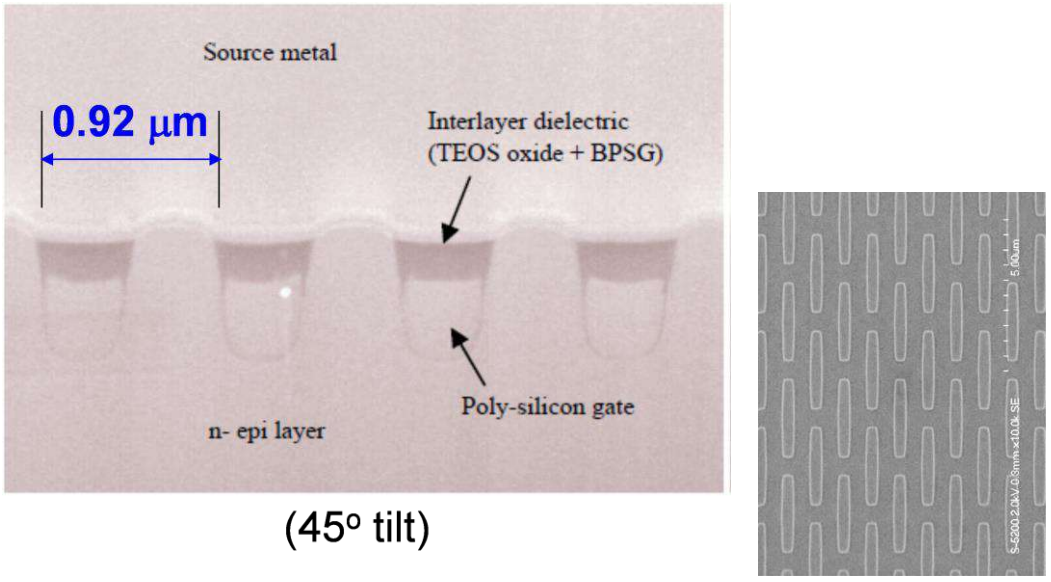


Fig. 2A

(i)

Fig. 2-21. Process flow of narrow pitch rectangular cell U-MOSFET. [42]

The cross-sectional SEM photograph of the fabricated 0.92-μm pitch U-MOSFET is shown in Fig. 2-22(a). The interlayer dielectric is filled inside trenches, which is slightly lower than silicon surface. Fig. 2-22(b) shows top view of the rectangular cells of the U-MOSFET.



(a) (b)

Fig. 2-22. SEM photograph of fabricated 0.92-μm pitch UMOSFET. (a) Cross-sectional view of an area including four trenches, observed by tilting angle of 45 degrees [40] © 2007 IEEE (modified), [41]. (b) Top view of plural rectangular cells.

Fig. 2-23 shows gate leakage current as a function of the gate electric field for single TEOS oxide and double layered oxide (TEOS and BPSG). The single TEOS oxide property was not satisfactory due to occurrence of a weak spot of reduced thickness. In contrast, in the case of the double oxide (TEOS and BPSG), ideal gate oxide properties were observed, i.e., small leakage current of 1 nA at 6.6 MV/cm and high breakdown electric field over 9.4 MV/cm. This demonstrates that the double oxide has a sufficient insulation capability.

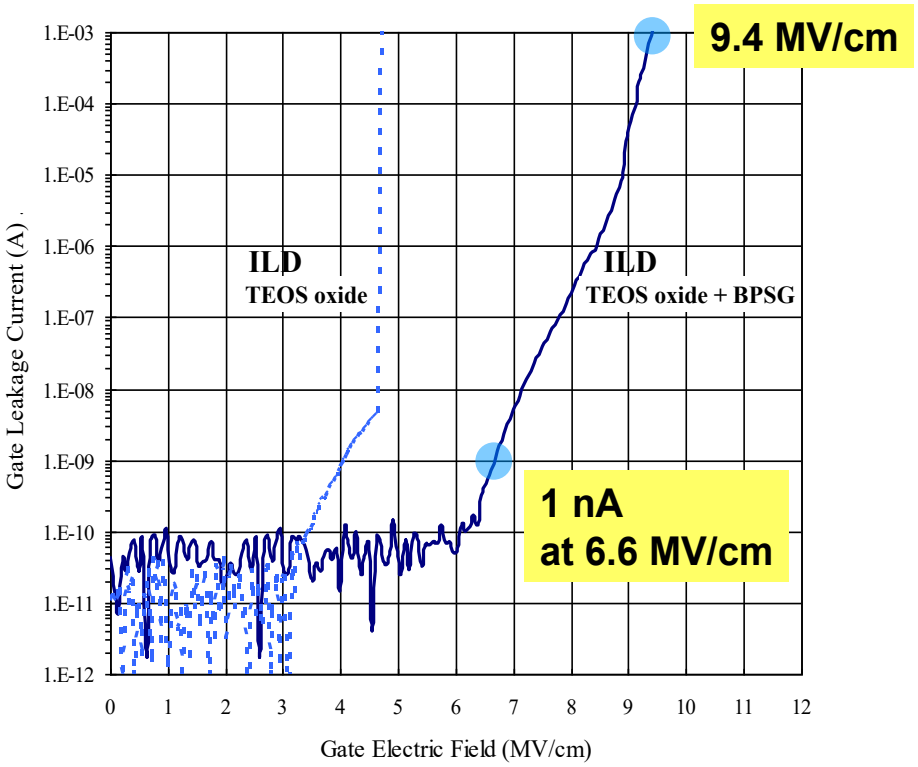


Fig. 2-23. Comparison of gate leakage current as a function of the gate electric field for fabricated UMOSFETs. [40] © 2007 IEEE (modified), [41]

2.3.4.3. Experimental results of device performance

A. On-resistance and principal characteristics

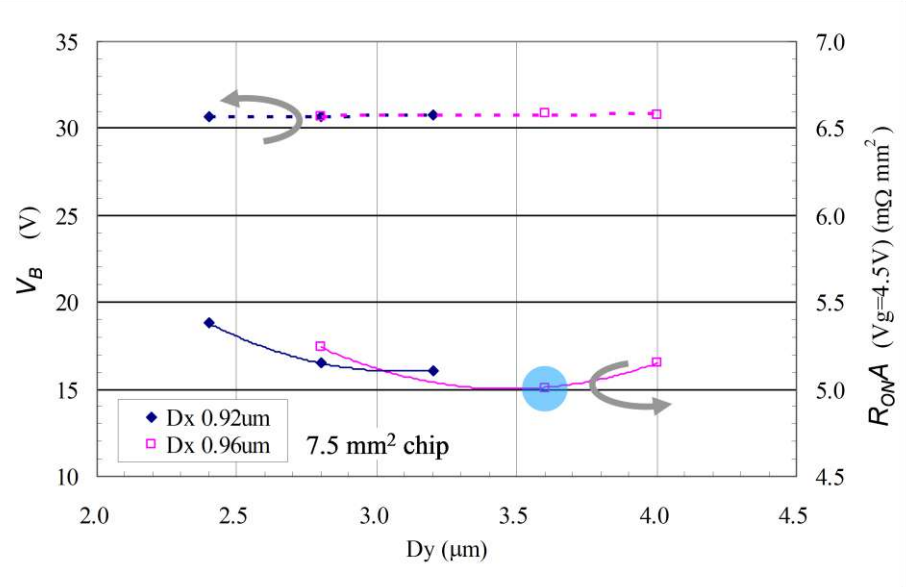
Fig. 2-24(a) and (b) show the cell dimension dependences of measured V_B and $R_{ON}A$ at V_{gs} = 4.5 V for the rectangular cell and the stripe cell, respectively. The V_B was over 30 V in all evaluated devices, and was independent of D_x and D_y.

The $R_{ON}A$ of the rectangular cell was saturated for larger D_y (at D_x = 0.92 μm and D_x = 0.96 μm). The tendency corresponded to the total channel width dependence shown in Fig. 2-18(a). The lowest $R_{ON}A$ of the rectangular cell was obtained at D_x = 0.96 μm and D_y = 3.6 μm. For this structure, the total channel width increased by 10% compared with that of the 2.0-μm square cell as shown in Fig. 2-18(a).

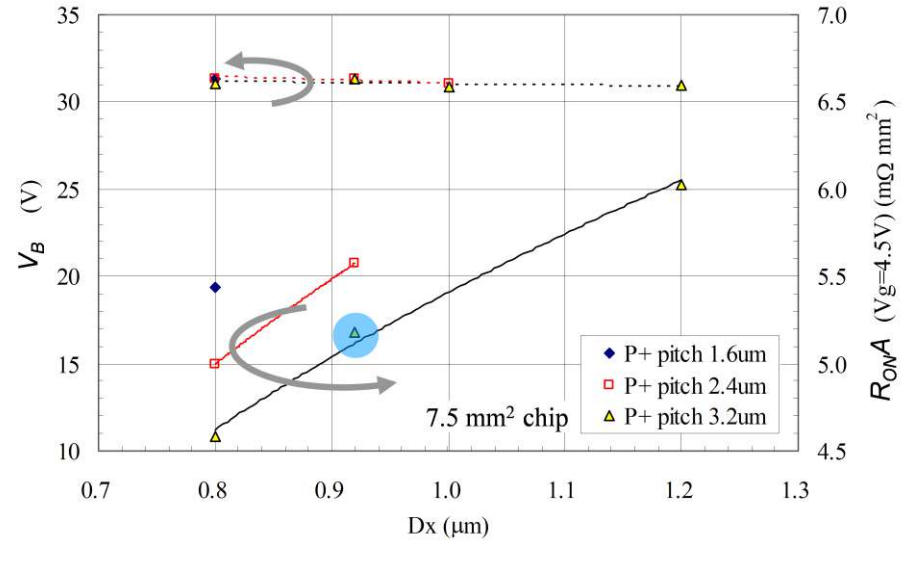
In the stripe cell, the $R_{ON}A$ decreased with decrease in D_y monotonously (for p^+–pitch of 3.2 μm and 2.4 μm). However, the $R_{ON}A$ of the stripe depended on the dimensions sensitively than that of the rectangular cell. It was found that the proposed rectangular cell has the advantages of process margin and $R_{ON}A$ stability over the stripe structure.

The principal characteristics of the rectangular cell and the stripe cell are shown in Table 2-6. The lowest $R_{ON}A$ of 4.3 mΩ·mm^2 at V_{gs} = 10 V and 5.0 mΩ·mm^2 at V_{gs} = 4.5 V were achieved in the rectangular cell with V_{TH} = 0.94 V and V_B = 30.5 V. For gate charge (Q_g), almost the same $R_{ON}\cdot Q_g$ performance was obtained for both structures.

In additionally fabricated rectangular cell U-MOSFET, the V_B of 39 V, $R_{ON}A$ of 8.1 mΩ·mm^2 at V_{gs} = 10 V, and 9.0 mΩ·mm^2 at V_{gs} = 4.5 V were obtained.



(a) Rectangular cell design



(b) Stripe cell design

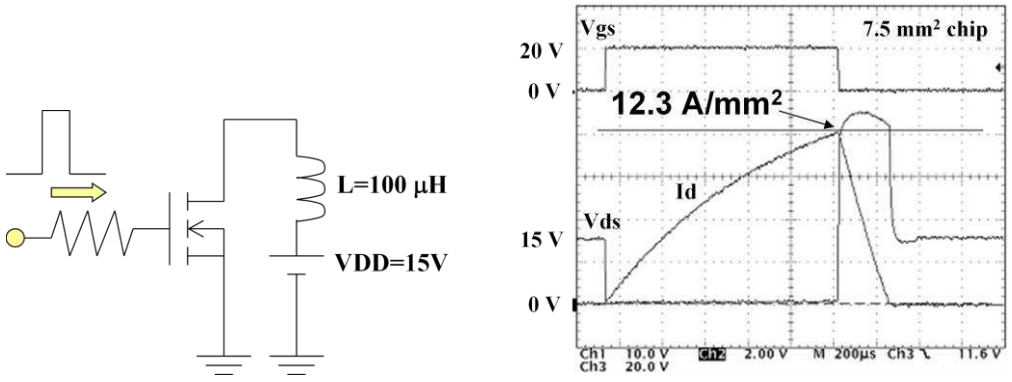
Fig. 2-24. Measured $R_{ON}A$ and V_B dependences on D_x, D_y and p$^+$–pitch. [40] © 2007 IEEE (modified), [41]

Table 2-6. Electrical characteristics of 30-V-class U-MOSFET for the rectangular cell and the stripe cell. [40] [41]

Symbol	Characteristics	Conditions	Rectangular cell	Stripe cell	Unit
V_B	Breakdown voltage	I_d = 250 μA	30.5	31.0	V
V_{TH}	Threshold voltage	V_{ds} = 10 V, I_d = 1mA	0.94	0.94	V
$R_{ON}A$	On-resistance	V_{gs} = 10 V	4.3	4.5	mΩ·mm²
$R_{ON}A$	On-resistance	V_{gs} = 4.5 V	5.0	5.3	mΩ·mm²
Q_g	Gate charge	V_{ds} = 15 V, V_{gs} = 5 V	9.8	9.5	nC/mm²
Q_{gd}	Gate–drain charge	V_{ds} = 15 V	4.1	3.6	nC/mm²
$R_{ON}\cdot Q_g$	FOM		42.1	42.8	mΩ·pF
$R_{ON}\cdot Q_{gd}$	FOM		17.6	16.2	mΩ·pF
R_g	Gate resistance		1.4	3.8	Ω

B. Avalanche capability

Fig. 2-25 shows waveforms of unclamped inductive switching (UIS) for fabricated rectangular cell U-MOSFET (D_x = 1.0 μm, D_y = 3.0 μm) with V_B of 39 V. In avalanche capability examination, sufficient current density over 12 A/mm² was confirmed, for D_x range of 0.8–1.0 μm and D_y range of 1.6–3.0 μm in the rectangular cell chip of 7.5 mm².



(a) (b)

Fig. 2-25. Avalanche capability of fabricated rectangular cell UMOSFET for D_x = 1.0 μm and D_y = 3.0 μm. (a) Test circuit of unclamped inductive switching (UIS). (b) Waveforms of UIS for L = 100 μH. [40] © 2007 IEEE (modified), [41]

2.3.5. Validation of on-resistance model

Fig. 2-26 shows the $R_{ON}A$ of developed 30-V-class U-MOSFET compared with that of both analytical model and TCAD simulation. The structural parameters, electrical parameters and physical constants are indicated in Table 2-7, Table 2-8 and Table 2-4. In the case of stripe cell that has continuous channel in longer direction of trench, the $R_{ON}A$ at V_{gs} = 4.5 V calculated by the model is 4.87 mΩ·mm^2, which corresponds to TCAD result of 4.82 mΩ·mm^2 very well.

When the developed U-MOSFET that has n^+/p^+ patterns alternately in longer direction of trench, the $R_{ON}A$, especially $R_{CH}A$, increases according to a ratio of n^+–length and p^+–pitch ($Ratio_{np}$). In the case of stripe cell with $Ratio_{np}$ = 0.7, the $R_{ON}A$ at V_{gs} = 4.5 V calculated by the model is 5.25 mΩ·mm^2, which corresponds to the experimental result of 5.2 mΩ·mm^2, with less than 1.0% error.

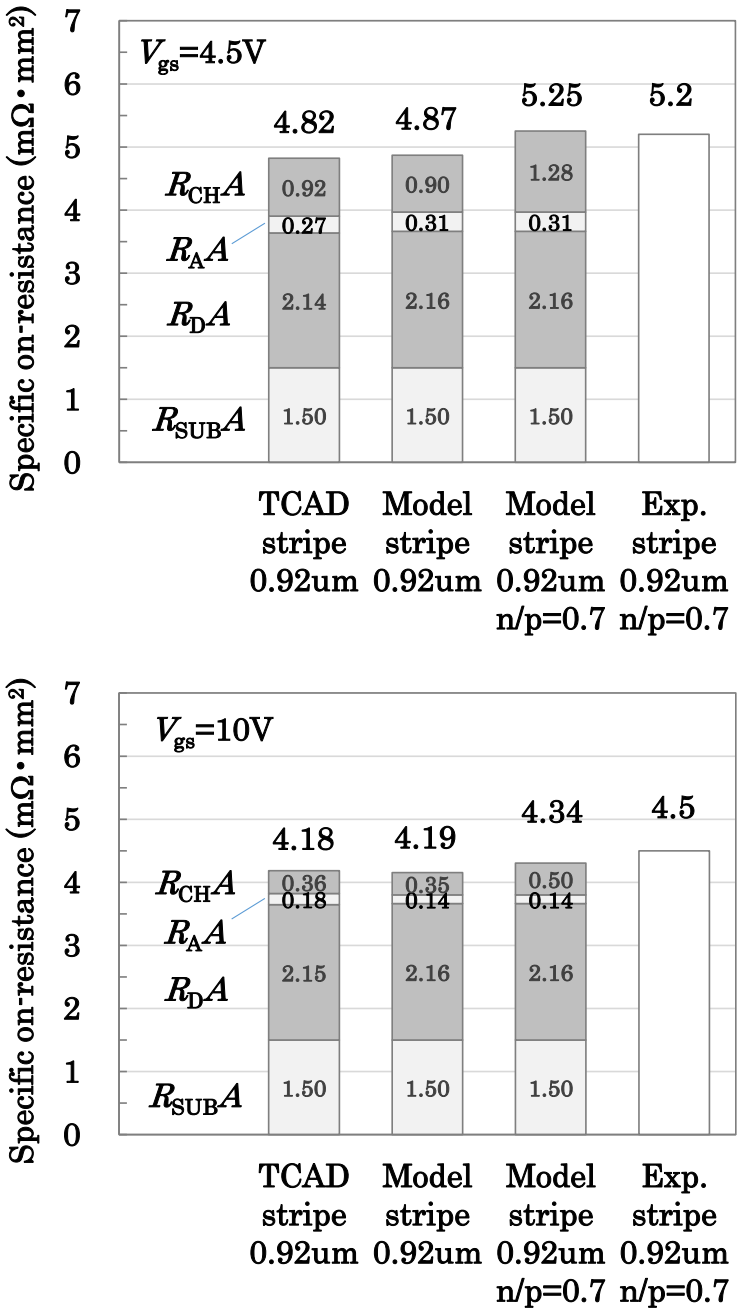


Fig. 2-26. Experimental results of $R_{ON}A$ for developed 30-V-class U-MOSFET compared with that of both analytical model and TCAD simulation. Under the condition of V_{gs} = 4.5 V, 10 V.

Table 2-7. Structural parameters of 30-V-class U-MOSFET to calculate $R_{ON}A$.

Symbol	Parameters	Numerics	Unit
W_{Cell}	Cell width	0.92	μm
W_T	Trench width	0.44	μm
W_{Mesa}	Mesa width	0.48	μm
D_T	Trench depth	1.00	μm
L_{CH}	Channel length	0.40	μm
L_A	Accumulation length	0.07	μm
K_A	Coefficient of current spreading in the accumulation region	0.60	
T_{GOX}	Gate oxide thickness	0.03	μm
X_{JS}	n^+–Source junction depth	0.50	μm
X_{JB}	p–Base junction depth	0.90	μm
p+ pitch	p^+–Pitch	3.20	μm
$Ratio_{np}$	Ratio of n^+–length / p^+–pitch	0.70	
L_D	n–Drift layer length	1.00	μm
ρ_D	Resistivity of n–drift layer	0.21	Ω・cm
N_D	Drift layer concentration	2.89×10^{15}	atoms/cm^3
T_{SUB}	n^+–Substrate thickness	100	μm
ρ_{SUB}	Resistivity of n^+–substrate	0.0015	Ω・cm
N_{SUB}	n^+–Substrate concentration	4.63×10^{19}	atoms/cm^3

Table 2-8. Electrical parameters of 30-V-class U-MOSFET to calculate $R_{ON}A$.

Symbol	Parameters	Numerics	Unit
V_{gs}	Gate–source voltage	4.5, 10	V
V_{TH}	Threshold voltage	0.94	V
μ_{ni}	Electron mobility of inversion layer	500	cm^2/Vs
μ_{na}	Electron mobility of accumulation layer	500	cm^2/Vs
μ_{n_D}	Electron mobility of n–drift layer	1000	cm^2/Vs
μ_{n_SUB}	Electron mobility of n^+–substrate	72	cm^2/Vs

2.4. Summary

In chapter 2, as improvement of the power loss for the LV-MOSFET, planar gate double-diffused MOSFET (D-MOSFET) and trench gate MOSFET (U-MOSFET) were described. The $R_{ON}A$ models of both D-MOSFETs and U-MOSFETs were detailed for two different surface patterns (stripe and square cell), respectively. In addition, each improvement structure, fabrication process, and evaluation result of the fabricated devices were described. In the validation of the $R_{ON}A$ models, the real device and calculated results by the model were compared for both 60-V D-MOSFET and 30-V U-MOSFET, and it was confirmed they showed good agreement.

As a summary of the development of the advanced low-power-loss MOSFETs, the performances are compared each other due to benchmarking of U-MOSFETs. The tradeoff between the V_B and the $R_{ON}A$ for 20–40-V-class U-MOSFETs is shown in Fig. 2-27. As reference line, one-dimensional (1-D) silicon-limit [11] is indicated. The developed rectangular cell U-MOSFETs' performances [40] [41] are superior to the published data [32] [33] [39] [43] [44] [45] [46] by approximately 30%.

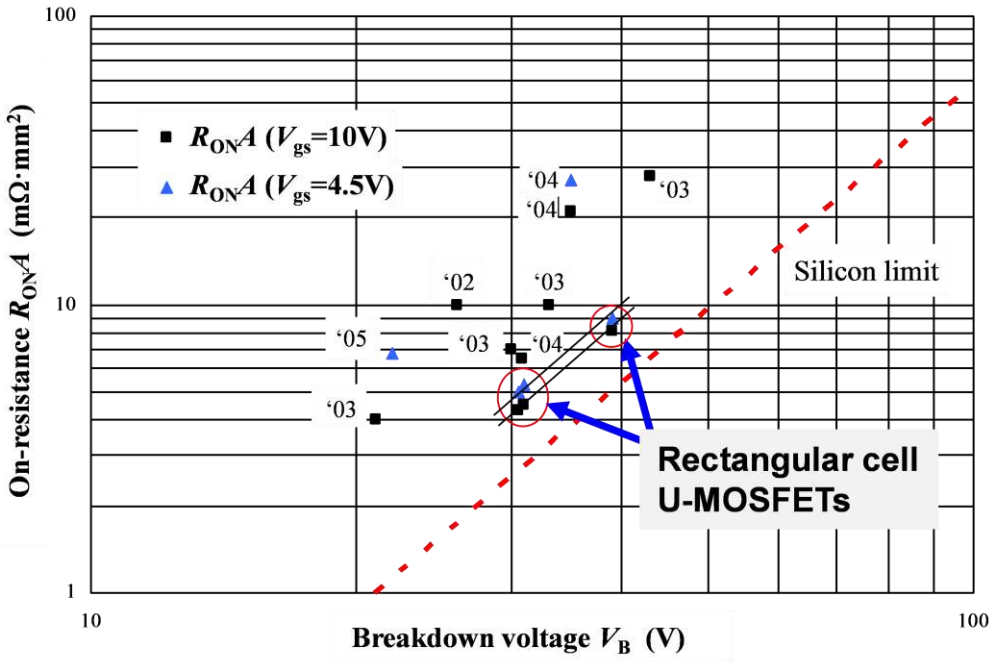


Fig. 2-27. Tradeoff between $R_{ON}A$ and V_B for U-MOSFETs by published data [32] [33] [39] [43] [44] [45] [46] and author's research [40] [41].

3. Development of Novel Charge Compensation Devices: SJ-UMOSFETs and FP-MOSFETs

3.1. Charge compensation structures for LV-MOSFETs

As great advancements of LV-MOSFETs in terms of performance, field-plate U-MOSFETs (FP-MOSFETs) [8] [47] [48] [49] [50] [51] [52] and superjunction U-MOSFETs (SJ-UMOSFETs) [53] [54] [55] [56] [57] were developed and commercialized in the early to mid-2000s.

The FP-MOSFETs applied fundamental technology called Reduced Surface Field (RESURF), which was devised for high-voltage lateral devices in 1979 [58] [59], to vertical direction. On the other hand, the theory of superjunction has been introduced in 1997 [60] and the SJ-MOSFET has firstly developed as HV-MOSFET, which was 600-V-class, by multiple-epitaxial technology [9]. After that the principle of superjunction applied to LV-MOSFETs, by changing the method to form the superjunction structure.

In both types of MOSFETs, on-resistance ($R_{ON}A$) could be drastically reduced with a high breakdown voltage (V_B) maintained. In particular, the FP-MOSFETs achieved not

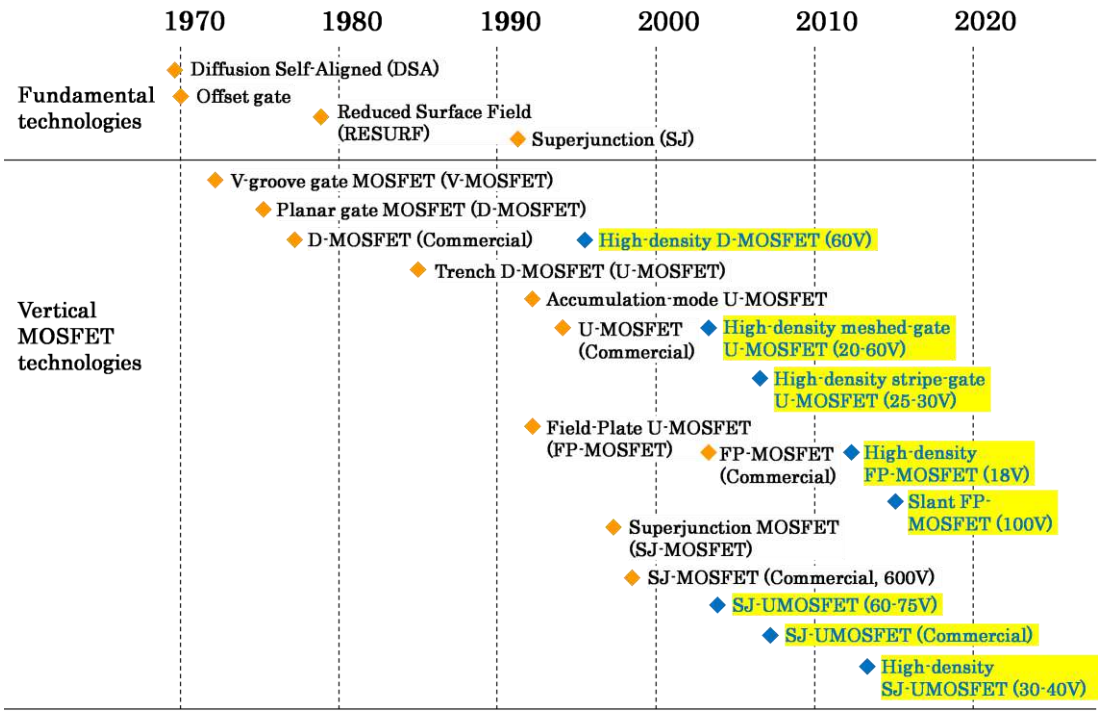


Fig. 3-1. Technology development history for vertical power MOSFETs. Highlights show author's research. (Re-publication of Fig. 2-1)

only ultralow $R_{ON}A$ but also very low reverse transfer capacitance (C_{rss}) and gate–drain charge (Q_{gd}) owing to the shielded-gate structure. Therefore, the FP-MOSFETs are currently the mainstream of high-performance applications and their advancement is continuing.

Fig. 3-1 shows technology development history of vertical power MOSFETs.

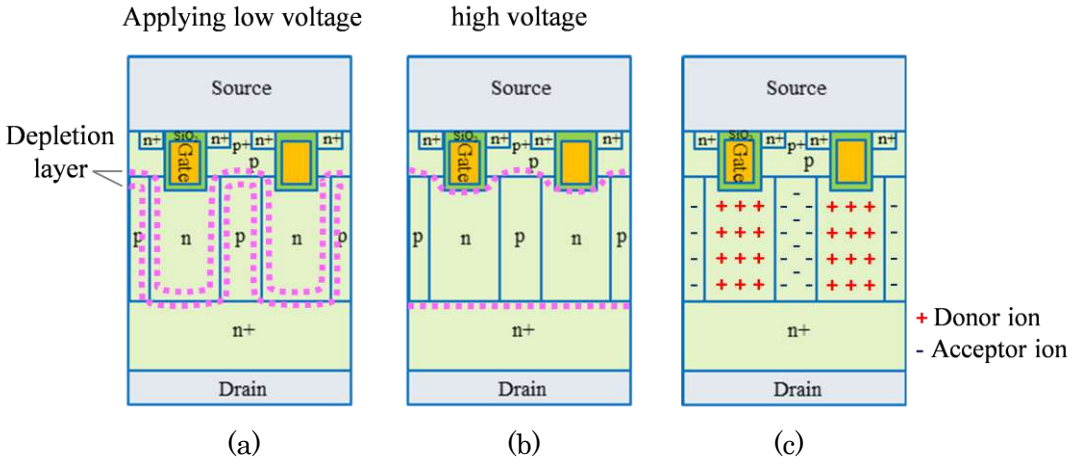


Fig. 3-2. Charge compensation for SJ-UMOSFET. Depletion layer formation when (a) low voltage and (b) high voltage are applying. (c) Charge compensation by p/n–columns.

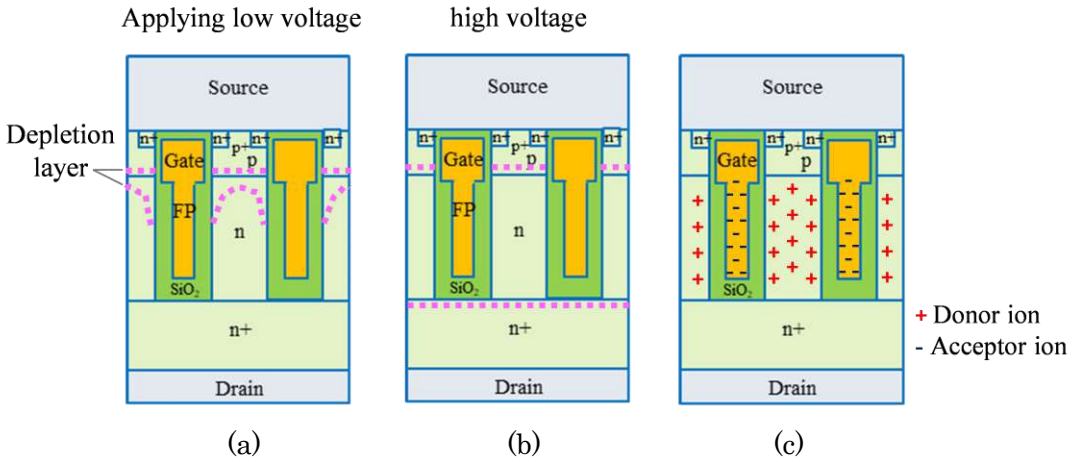


Fig. 3-3. Charge compensation for FP-MOSFET. Depletion layer formation when (a) low voltage and (b) high voltage are applying. (c) Charge compensation by using field-plate.

3.1.1. Basic principles of superjunction devices.

Superjunction structure has been originally proposed for high-voltage devices, and the (high-voltage) SJ-MOSFET structure actually achieved the significant improvement of tradeoff between $R_{ON}A$ and V_B [60] [9], which exceeded 1-D silicon-limit [11].

Fig. 3-2(a)–(c) explains charge compensation principle in the (low-voltage) SJ-UMOSFET structure. In this structure, p–columns and n–columns are alternately arranged in the drift layer in lateral direction. When a voltage is applied to the drain electrode, boundaries of each p/n–column begin to form the depletion layer in a low voltage (Fig. 3-2(a)) and full depletion layer is formed with increasing the voltage (Fig. 3-2(b)). At the time, charge in the drift layer is compensated between the p/n–columns (Fig. 3-2(c)). Thus, high V_B is guaranteed even in a high n–column layer impurity concentration for the superjunction structure.

Due to the fully-depleted drift layer, an ideal V_B of the SJ-UMOSFET (which is same as that of the SJ-MOSFET) can be given by simplified expression.

$$V_B(\text{ideal, SJ}) \approx E_C T_{SJ} \tag{3-1}$$

Here, E_C is a critical electric field and T_{SJ} is a thickness of the p/n–column. To simplify calculation of the drift layer resistance (R_DA), it assumes both width of p–column (W_P) and n–column (W_N) are same. Then an ideal R_DA is expressed as

$$R_D\text{A(ideal, SJ)} \approx \frac{2T_{SJ}}{q\mu_e N_D}, \tag{3-2}$$

where q is the elementary charge, N_D is the n–column layer concentration, and μ_e is electron mobility in the n–column layer. Meanwhile the charge balance condition between the p/n–columns and the optimum charge density, which is lead from Poisson's equation, are given by the following [11] [59] [60].

$$N_D \frac{W_N}{2} = N_A \frac{W_P}{2} = \frac{\varepsilon_{Si}\varepsilon_0 E_C}{q} \tag{3-3}$$

Here N_A is the p–column layer concentration and $\varepsilon_{Si}\varepsilon_0$ is the permittivity of silicon. By substituting Eqs. (3-1) and (3-3) into Eq. (3-2), the ideal R_DA can be obtained

$$R_D\text{A(ideal, SJ)} \approx \frac{V_B W_N}{\mu_e \varepsilon_{Si}\varepsilon_0 {E_C}^2}. \tag{3-4}$$

3.1.2. Basic principles of field-plate devices

Field-plate technology bases on the RESURF principle [58] [59], and the FP-MOSFET is applying it in each unit cell structure in vertical direction. The FP-MOSFET has also achieved the significant improvement of tradeoff between $R_{ON}A$ and V_B in under the 100-V-class [50] [51], which exceeded 1-D silicon-limit [11].

Fig. 3-3(a)–(c) explains charge compensation principle in the FP-MOSFET structure. When a voltage is applied to the drain electrode, the field-plate inside the trench gives electric field effect to silicon mesa region through thick oxide. Therefore, in a low voltage, the depletion layer expands from both boundaries of pn-junction and oxide/silicon mesa (Fig. 3-3(a)). Then, full depletion layer is formed with increasing the voltage (Fig. 3-3(b)). At the time, charge in the drift layer is compensated by the field-plate [61] (Fig. 3-3(c)). Thus, like the SJ-UMOSFET, high V_B is guaranteed even in a high n–drift layer impurity concentration for the FP-MOSFET structure.

Due to the fully-depleted drift layer, an ideal V_B of the FP-MOSFET can be given by simplified expression.

$$V_B(\text{ideal, FP}) \approx E_C L_D \tag{3-5}$$

Here, L_D is a length of the n–drift layer. To simplify calculation of the drift layer resistance (R_DA), it assumes both width of trench (W_T) and silicon mesa (W_{Mesa}) are same. Then an ideal R_DA is expressed as

$$R_D\text{A(ideal, FP)} \approx \frac{2L_D}{q\mu_e N_D}, \tag{3-6}$$

The charge balance condition of the FP-MOSFET is accomplished by the optimum charge density, which is lead from Poisson's equation, and is given by the following [11] [59] [60].

$$N_D \frac{W_{Mesa}}{2} = \frac{\varepsilon_{Si}\varepsilon_0 E_C}{q} \tag{3-7}$$

By substituting Eqs. (3-5) and (3-7) into Eq. (3-6), the ideal R_DA can be obtained

$$R_D\text{A(ideal, FP)} \approx \frac{V_B W_{Mesa}}{\mu_e \varepsilon_{Si}\varepsilon_0 {E_C}^2}. \tag{3-8}$$

3.2. Superjunction U-MOSFET (SJ-UMOSFET) featuring a low-voltage device

3.2.1. Basic structure and on-resistance ($R_{ON}A$) components of SJ-UMOSFET

Schematic cross-sectional structure of SJ-UMOSFET for two unit-cells area is shown in Fig. 3-4. Fig. 3-4(a) shows a distribution of electric field E_y of drift layer in vertical direction y, when a reverse bias applies to the drain. In an ideal SJ-UMOSFET, the E_y is distributed like a trapezoid and a critical electric field E_C is nearly uniform, which are different from those of the D-MOSFET or the U-MOSFET. V_B of two-dimensional superjunction is determined by the area of this electric field and is given by

$$V_B \approx \int_0^{L_{dep}} E_y dy. \tag{3-9}$$

Here L_{dep} is depletion layer length in y. In assumption, if a depletion layer length in the p–base region is negligible, the V_B of SJ-UMOSFET is approximated as

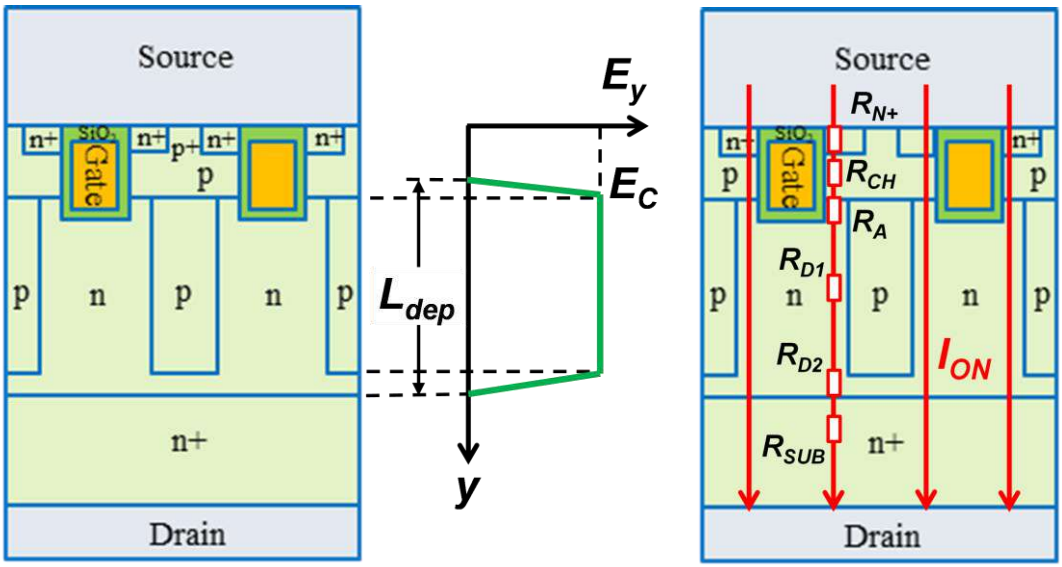
$$V_B \approx E_C\left(T_{SJ} - T_{BUF}\right) + \frac{1}{2}E_C T_{BUF}, \tag{3-10}$$

where T_{SJ} is p–column thickness and T_{BUF} is buffer layer thickness under the p–column, which shares a part of the V_B. The V_B of SJ-UMOSFET is independent from N_D, which is different from the case of the D-MOSFET or the U-MOSFET. The V_B and the R_{DA} has a nearly linear relationship that is described as $R_{DA} \propto V_B^{1.1}$ in [60].

Fig. 3-4(b) shows on-state current paths and on-resistance components of SJ-UMOSFET. The R_{N+A} is negligible as well as that of U-MOSFET. The R_{ONA} of SJ-UMOSFET ($R_{ON}{}^{SJUMOS}A$) can be approximated by using main components,

$$R_{ON}{}^{SJUMOS}\mathrm{A} \approx R_{CH}A + R_A A + R_{D1}A + R_{D2}A + R_{SUB}A. \tag{3-11}$$

In Eq. (3-11), R_{CHA} and R_{AA} are divided into three cases, i.e., the SJ-UMOSFET design is stripe geometry, square cell geometry, or square p–column in stripe trench. Fig. 3-5(a) shows structural parameters of SJ-UMOSFET. As shown in Fig. 3-5(b) and Fig. 3-5(c), channel width per unit area "A" is shown as $2W_{Cell}/{W_{Cell}}^2 = 2/W_{Cell}$ in stripe cell design, or $4W_{Mesa}/{W_{Cell}}^2$ in square cell design. Here, W_{Cell} is cell width and W_{Mesa} is mesa width.



(a) (b)

Fig. 3-4. Schematic cross-sectional structures of SJ-UMOSFET, which shows two unit-cells area. (a) Electric field distribution in vertical direction of off-state. (b) On-state current paths and components of on-resistance.

$R_{CH}A$, R_AA and $R_{SUB}A$ in Eq. (3-11) are expressed by analytical model as below.

$$R_{CH}\mathrm{A} = \begin{cases} \dfrac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}, & \text{in stripe cell} \\ \dfrac{L_{CH}W_{Cell}}{2\mu_{ni}C_{gox}(V_{gs}-V_{TH})}, & \text{in stripe cell (square p} - \text{column)} \\ \dfrac{L_{CH}{W_{Cell}}^2}{4W_{Mesa}\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}, & \text{in square cell} \end{cases} \tag{3-12}$$

$$R_A\mathrm{A} = \begin{cases} K_A\dfrac{(2L_A+W_T)W_{Cell}}{4\mu_{na}C_{GOX}V_{gs}}, & \text{in stripe cell} \\ K_A\dfrac{(2L_A+W_T)W_{Cell}}{4\mu_{na}C_{GOX}V_{gs}}, & \text{in stripe cell (square p} - \text{column)} \\ K_A\dfrac{(2L_A+W_T){W_{Cell}}^2}{8W_{Mesa}\mu_{na}C_{GOX}V_{gs}}, & \text{in square cell} \end{cases} \tag{3-13}$$

$$R_{SUB}\mathrm{A} = \rho_{SUB}T_{SUB} \tag{3-14}$$

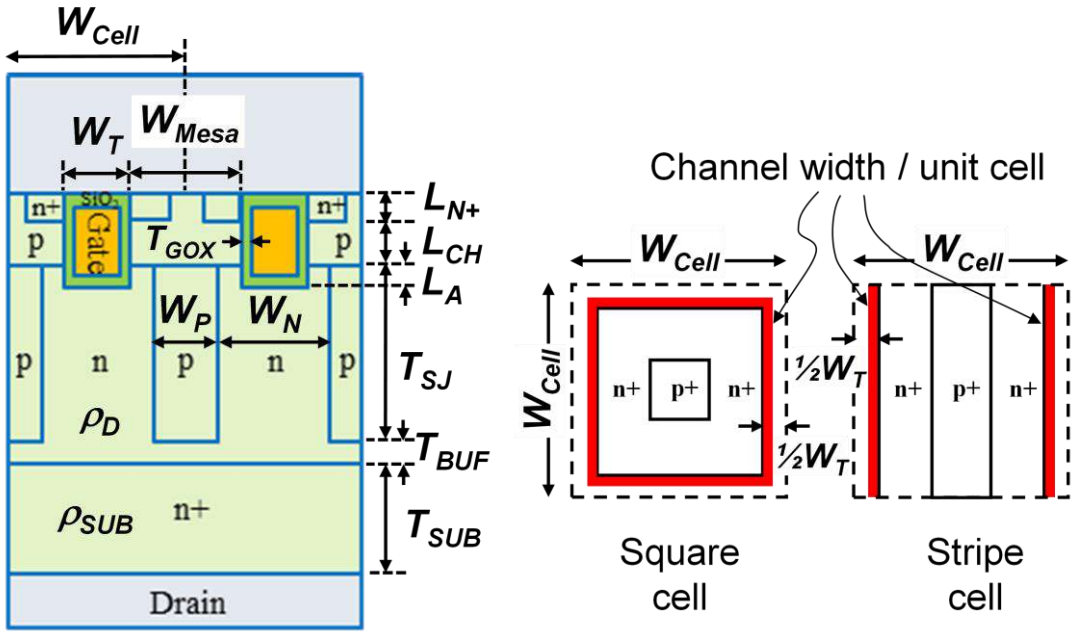


Fig. 3-5. (a) Structural parameters of SJ-UMOSFET. Top view of SJ-UMOSFET unit-cell layout for (b) square cell design and (c) stripe cell design.

Here, W_T is trench width and other same symbols are the same as those of subsection 2.2.1, i.e., L_{CH} is channel length, L_A is accumulation length, ρ_{SUB} is resistivity of n^+–substrate, T_{SUB} is thickness of the n^+–substrate, μ_{ni} is electron mobility of inversion layer, μ_{na} is electron mobility of accumulation layer, C_{GOX} is gate oxide capacitance, V_{gs} is gate voltage, and V_{TH} is threshold voltage. K_A is a coefficient of considering current spreading from the accumulation region to the drift region [25] [26]. In Eq. (3-13), the total accumulation length of the unit cell is given by $2L_A + W_T$. K_A is assumed to be around 0.7.

In addition, $R_{D1}A$ and $R_{D2}A$ in Eq. (3-11) are also divided into three cases, i.e., the SJ-UMOSFET design is stripe geometry, square cell geometry or square p–column in stripe trench. By using other components which are $R_{D\_P}A$, $R_{D\_T}A$ and $R_{D\_N}A$ as shown in Fig. 3-6 and Fig. 3-7, R_DA is expressed by analytical model as below.

$$R_D\mathrm{A} = R_{D1}\mathrm{A} + R_{D2}\mathrm{A} \tag{3-15}$$

$$R_D\mathrm{A} = \begin{cases} R_{D\_P}\mathrm{A}, & \text{in stripe cell} \\ \dfrac{R_{D\_N}A \cdot R_{D\_P}A}{R_{D\_N}A + R_{D\_P}A}, & \text{in stripe cell (square p} - \text{column)} \\ \dfrac{R_{D\_T}A \cdot R_{D\_P}A}{R_{D\_T}A + R_{D\_P}A}, & \text{in square cell} \end{cases} \tag{3-16}$$

$$R_{D\_P}\mathrm{A} = \begin{cases} R_{D1\_P}\mathrm{A} + R_{D2\_P}\mathrm{A}, & \text{in stripe cell} \\ \dfrac{W_{Cell}}{W_P}\left(R_{D1\_P}\mathrm{A} + R_{D2\_P}\mathrm{A}\right), & \text{in stripe cell (square p} - \text{column)} \\ \dfrac{{W_{Cell}}^2}{{W_{Cell}}^2 - {W_T}^2}\left(R_{D1\_P}\mathrm{A} + R_{D2\_P}\mathrm{A}\right), & \text{in square cell} \end{cases} \tag{3-17}$$

$$\begin{aligned} R_{D1\_P}\mathrm{A} = {} & \frac{\rho_D W_{Cell}}{2} \ln \frac{W_N - W_{dep\_N}}{W_T} \\ & + \frac{\rho_D W_{Cell}}{W_N - W_{dep\_N}} \left(T_{SJ} - L_A - \frac{W_{Mesa} - W_P - W_{dep\_N}}{2} \right) \end{aligned} \tag{3-18}$$

$$R_{D2\_P}\mathrm{A} = \frac{\rho_D W_{Cell}}{2} \ln \frac{W_{Cell}}{W_N - W_{dep\_N}} + \rho_D \left(T_{BUF} - \frac{W_P + W_{dep\_N}}{2} \right) \tag{3-19}$$

$$R_{D\_T}\mathrm{A} = \frac{{W_{Cell}}^2}{{W_T}^2} \rho_D \left(T_{SJ} - L_A + T_{BUF} \right) \tag{3-20}$$

$$R_{D\_N}\mathrm{A} = \frac{W_{Cell}}{W_N - W_{dep\_N}} \left[\frac{\rho_D W_{Cell}}{2} \ln \frac{W_{Cell}}{W_T} + \rho_D \left(T_{SJ} - L_A - \frac{W_{Mesa}}{2} + T_{BUF} \right) \right] \tag{3-21}$$

Here, ρ_D is resistivity of n–drift layer, W_P is p–column width and W_N is n–column width which equals to a distance between p–columns. Moreover, W_{dep_N} is depletion layer width at p–column/n–column junction and is given by

$$W_{dep\_N} = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0 (V_{bi} + V_{ON})}{q} \left[\frac{N_A}{N_D (N_A + N_D)} \right]}, \tag{3-22}$$

where q is the elementary charge, $\varepsilon_{Si}\varepsilon_0$ is the permittivity of silicon, V_{bi} is built-in potential at the pn-junction, V_{ON} is on-state voltage, N_D is n–drift layer concentration and N_A is p–column layer concentration.

In stripe cell, the $R_{D}A$ is series resistance of $R_{D1\_P}A$ and $R_{D2\_P}A$, as expressed in Eqs. (3-16)–(3-19), and shown in Fig. 3-4(b). The $R_{D1\_P}A$ is a drift layer resistance between p–columns, which is spreading from under the trench to p–columns. The $R_{D2\_P}A$ is a buffer layer resistance, which is spreading to under p–columns.

In square cell, the $R_{D}A$ is parallel resistance of $R_{D\_P}A$ and $R_{D\_T}A$, as expressed in Eqs. (3-16)–(3-20), and shown in Fig. 3-6(a). The $R_{D\_P}A$ is a part of drift layer resistance which is between p–columns, as shown in Fig. 3-7(b). The $R_{D\_T}A$ is another part of drift layer resistance which is under trench intersection, as shown in Fig. 3-6(c).

In stripe cell with square p–column, the $R_{D}A$ is parallel resistance of $R_{D\_P}A$ and $R_{D\_N}A$, as expressed in Eqs. (3-16)–(3-19) and (3-21), and shown in Fig. 3-7(a). The $R_{D\_P}A$ is a part of drift layer resistance which is between p–columns under the trench, as shown in Fig. 3-7(b). The $R_{D\_N}A$ is remaining part of drift layer resistance, as shown in Fig. 3-7(c).

To improve the $R_{ON}{}^{SJUMOS}A$ with necessary V_B maintained, all the components of $R_{ON}{}^{SJUMOS}A$ have to be reduced by individual appropriate techniques.

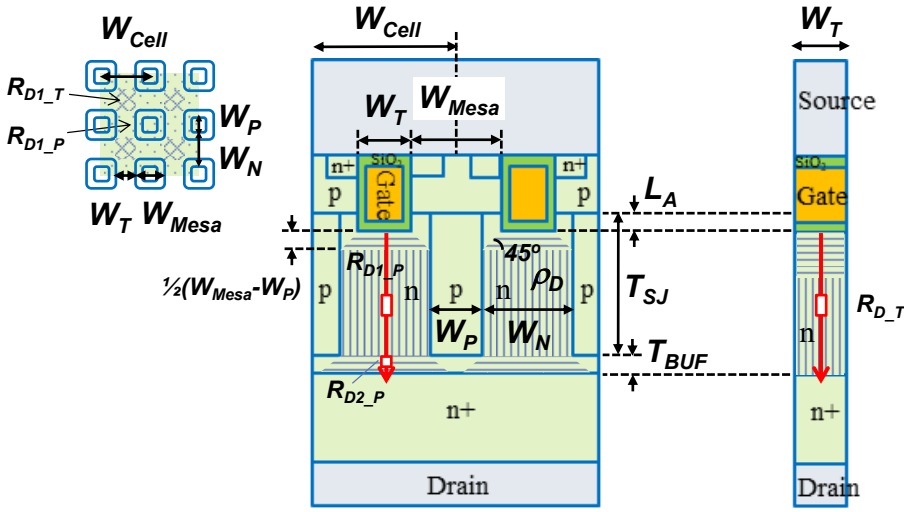


Fig. 3-6. (a) Top view of SJ-UMOSFET for square cell layout. Schematic cross-sectional structure, which shows components of the n–drift layer resistance (R_{D1_P}, R_{D2_P}, R_{D_T}). (b) Current flow spreading in 45 degrees from four sides surrounding the square p–column. (c) Current flow under trench intersection.

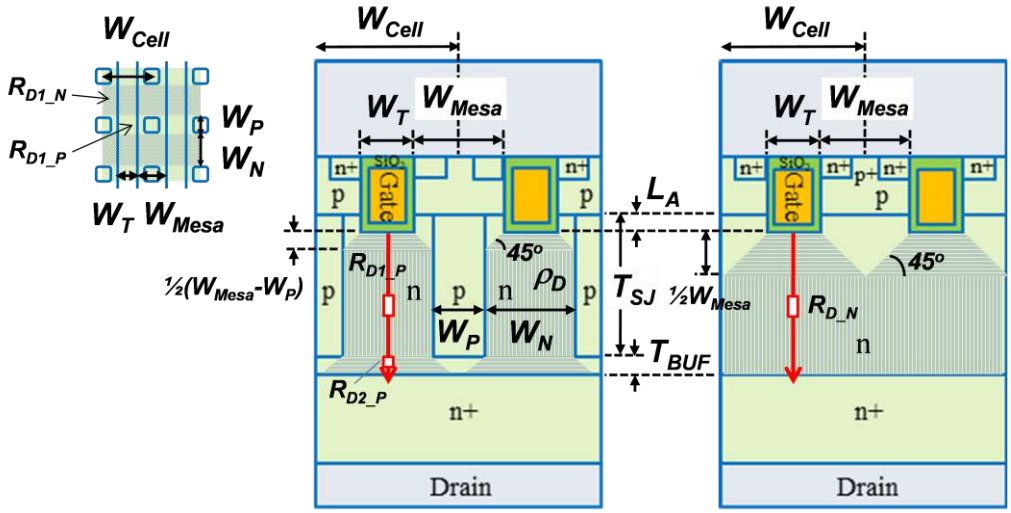


Fig. 3-7. (a) Top view of SJ-UMOSFET for square p–column in stripe cell layout. Schematic cross-sectional structure, which shows components of the n–drift layer resistance (R_{D1_P}, R_{D2_P}, R_{D_N}). (b) Current flow spreading in 45 degrees from both sides of the square p–column. (c) Current flow spreading in 45 degrees in n–drift region.

3.2.2. List of on-resistance model

Table 3-1. List of $R_{ON}A$ model equations for SJ-UMOSFET (stripe and square cell design).

Stripe	Square cell
$R_{CH}\mathrm{A} = \dfrac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}$	$R_{CH}\mathrm{A} = \dfrac{L_{CH}{W_{Cell}}^2}{4W_{Mesa}\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}$
$R_A\mathrm{A} = K_A\dfrac{(2L_A+W_T)W_{Cell}}{4\mu_{na}C_{GOX}V_{gs}}$	$R_A\mathrm{A} = K_A\dfrac{(2L_A+W_T){W_{Cell}}^2}{8W_{Mesa}\mu_{na}C_{GOX}V_{gs}}$
$R_D\mathrm{A} = R_{D1\_P}\mathrm{A} + R_{D2\_P}\mathrm{A}$	$R_D\mathrm{A} = \dfrac{R_{D\_T}A\cdot R_{D\_P}A}{R_{D\_T}A + R_{D\_P}A}$
$R_{D1\_P}\mathrm{A} = \dfrac{\rho_D W_{Cell}}{2}\ln\dfrac{W_N-W_{dep\_N}}{W_T} + \dfrac{\rho_D W_{Cell}}{W_N-W_{dep\_N}}\left(T_{SJ}-L_A - \dfrac{W_{Mesa}-W_P-W_{dep\_N}}{2}\right)$	$R_{D\_T}\mathrm{A} = \dfrac{{W_{Cell}}^2}{{W_T}^2}\rho_D(T_{SJ}-L_A+T_{BUF})$
$R_{D2\_P}\mathrm{A} = \dfrac{\rho_D W_{Cell}}{2}\ln\dfrac{W_{Cell}}{W_N-W_{dep\_N}} + \rho_D\left(T_{BUF}-\dfrac{W_P+W_{dep\_N}}{2}\right)$	$R_{D\_P}\mathrm{A} = R_{D1\_P}\mathrm{A} + R_{D2\_P}\mathrm{A}$
	$R_{D1\_P}\mathrm{A} = \dfrac{\rho_D W_{Cell}}{2}\ln\dfrac{W_N-W_{dep\_N}}{W_T} + \dfrac{\rho_D W_{Cell}}{W_N-W_{dep\_N}}\left(T_{SJ}-L_A - \dfrac{W_{Mesa}-W_P-W_{dep\_N}}{2}\right)$
	$R_{D2\_P}\mathrm{A} = \dfrac{\rho_D W_{Cell}}{2}\ln\dfrac{W_{Cell}}{W_N-W_{dep\_N}} + \rho_D\left(T_{BUF}-\dfrac{W_P+W_{dep\_N}}{2}\right)$
$R_{SUB}\mathrm{A} = \rho_{SUB}T_{SUB}$	$R_{SUB}\mathrm{A} = \rho_{SUB}T_{SUB}$

Table 3-2. List of $R_{ON}A$ model equations for SJ-UMOSFET (square p–column in stripe trench).

Stripe (square p–column)
$R_{CH}\mathrm{A} = \dfrac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}$
$R_{A}\mathrm{A} = K_A\dfrac{(2L_A+W_T)W_{Cell}}{4\mu_{na}C_{GOX}V_{gs}}$
$R_{D}\mathrm{A} = \dfrac{R_{D\_N}A\cdot R_{D\_P}A}{R_{D\_N}A+R_{D\_P}A}$
$R_{D\_N}\mathrm{A} = \dfrac{W_{Cell}}{W_N-W_{dep\_N}}\left[\dfrac{\rho_D W_{Cell}}{2}\ln\dfrac{W_{Cell}}{W_T}+\rho_D\left(T_{SJ}-L_A-\dfrac{W_{Mesa}}{2}+T_{BUF}\right)\right]$
$R_{D\_P}\mathrm{A} = R_{D1\_P}\mathrm{A}+R_{D2\_P}\mathrm{A}$
$R_{D1\_P}\mathrm{A} = \dfrac{\rho_D W_{Cell}}{2}\ln\dfrac{W_N-W_{dep\_N}}{W_T}+\dfrac{\rho_D W_{Cell}}{W_N-W_{dep\_N}}\left(T_{SJ}-L_A-\dfrac{W_{Mesa}-W_P-W_{dep\_N}}{2}\right)$
$R_{D2\_P}\mathrm{A} = \dfrac{\rho_D W_{Cell}}{2}\ln\dfrac{W_{Cell}}{W_N-W_{dep\_N}}+\rho_D\left(T_{BUF}-\dfrac{W_P+W_{dep\_N}}{2}\right)$
$R_{SUB}\mathrm{A} = \rho_{SUB}T_{SUB}$

3.2.3. 60-V narrow pitch SJ-UMOSFET applying multiple-ion-implantation [2]

The $R_{ON}A$ of the LV-MOSFET can be drastically reduced by adopting superjunction (SJ) consisting of repeated deep p/n–columns [62] [63]. For the superjunction structures satisfying charge balance condition, the higher performance is obtained for the narrower pn-junction pitch. However, in the conventional D-MOSFETs with narrow cell pitch, the merit of the superjunction introduction would be reduced, because the $R_{JFET}A$ becomes dominant as the cell pitch is scaled down.

In this subsection, the superjunction concept combined with the U-MOSFET, which is ideal structure for future scaling, is described [10] [64]. The superjunction structure with deep p–columns is formed by multiple boron implantations with varied energies up to 2.0 MeV. This technique enables to make narrow pitch pn-junctions, which are favorable to reduce the $R_{ON}A$.

Firstly, simulated properties of the multiple boron implantations are described, followed by electrical characteristics of the simulated SJ-diodes and SJ-UMOSFETs. Then, the experimental results on the fabricated SJ-diodes is presented. Finally, the performance of the proposed SJ-UMOSFETs is demonstrated.

3.2.3.1. Unit-cell structure design and device simulation

Schematic cross-sectional structures of the basic unit cell for the SJ-UMOSFETs are shown in Fig. 3-8(a) and (b). The p–columns are formed in n–epitaxial layer (n–epi layer) by high energy boron ion implantations through mask windows. The ions are injected vertically to the silicon wafers. The implantation process is divided into multiple injections with different energies up to maximum value of 2.0 MeV. Depending on the number of the boron ion implantations, three types of structures, which is single p–column, split p–column, or continuous p–column, can be fabricated, as shown in Fig. 3-9.

In the case of the split p–column or the continuous p–column, the middle energies are chosen to equalize peak separation in the boron doping profile. The resultant p–column region is 2.5–3.0-μm deep and 1.0–2.0-μm wide, depending on the mask window widths and the maximum implantation energies. The impurity concentrations in the n–epi layer and the boron dose are varied to optimize charge balance between the depleted n– and p–regions under reverse biases.

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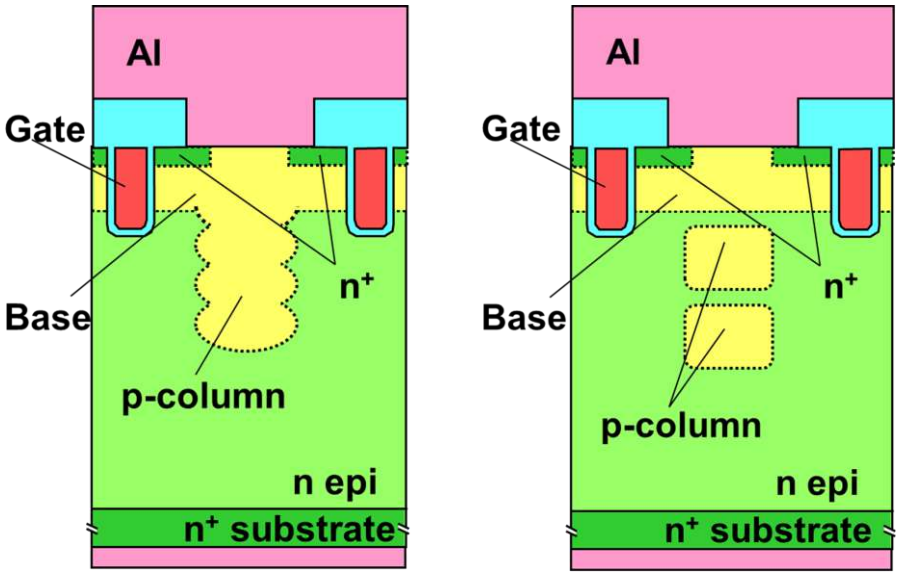
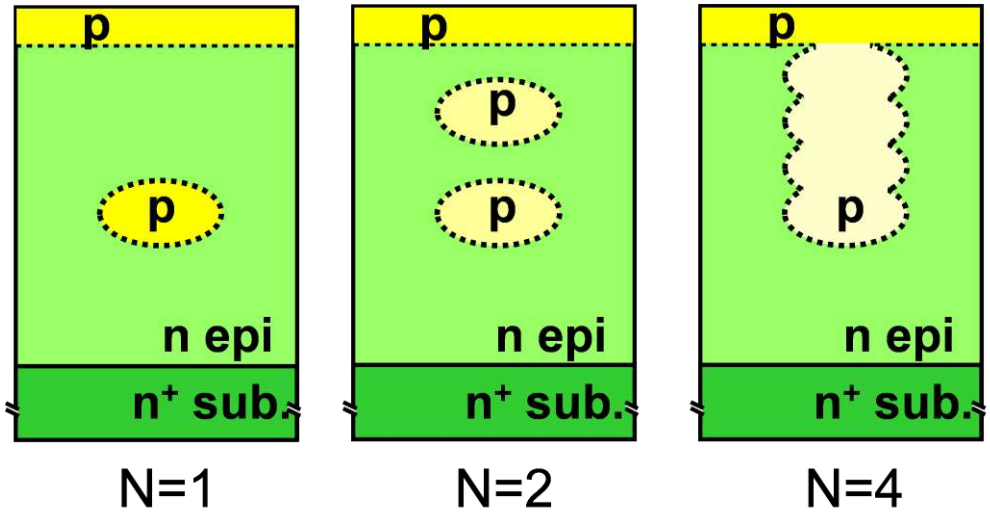
[2] Subsection 3.2.3 is reconstruction of [10] chapter II–IV, © 2004 IEEE, and [64] chapter II–IV, © 2005 IEEE. A part of description is modified and comprehensive explanations are additionally provided.



(a) Number of p–columns N= 4. (b) Number of p–columns N= 2.

Fig. 3-8. Schematic cross-sectional structures of developed SJ-UMOSFETs fabricated by using multiple-ion-implantation. (a) Continuous p–column [10] © 2004 IEEE (modified). (b) Split p–column [64] © 2005 IEEE (modified).



(a) Single p–column. (N= 1)

(b) Split p–column. (N= 2)

(c) Continuous p–column. (N= 4).

Fig. 3-9. Number of the ion-implantations for SJ-UMOSFETs fabrication.

To evaluate the properties of the present superjunction structures, process and device simulations are performed. The Monte Carlo method is used to simulate the boron implantations for deep p–column formation.

The V_B dependence on boron doping profile was investigated for two-dimensional SJ-diode structures. The profile is changed by number of boron injections, defined by N, keeping the total dose constant. In evaluating the SJ-UMOSFET performance, superjunction structures are added to the optimized U-MOSFET structures, which have a cell size of 3.0 or 4.0 μm.

Fig. 3-10 shows boron doping profiles along the center of the p–column. For a single injection (N = l), the boron doping profile has a peak at 2.5 μm in depth. As the number of injections increases, the profile gets more uniform, as expected.

Fig. 3-11 shows the dependence of the V_B on the number of injections. The V_B increases rapidly from N = 0 (non-SJ) to N = 2, while it saturates for $N \geq 3$. This result means that the boron profile for N = 4 in Fig. 3-10 is sufficiently uniform to achieve a maximum V_B under a given charge balance condition. It would be appropriate to set N = 2–4 to reduce the cost performance in the SJ-UMOSFET fabrication processes.

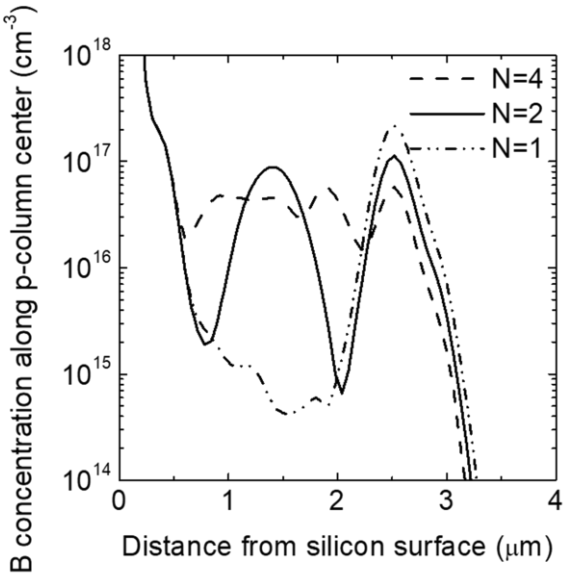


Fig. 3-10. Simulated boron doping profiles along the p–column center. The profiles for different number of boron injections are compared. [64] © 2005 IEEE (modified).

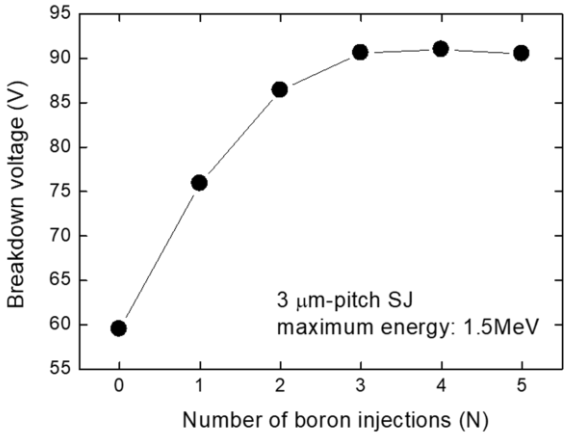


Fig. 3-11. Dependence of the simulated V_B on the number of boron injections for a constant total dose of 1.2×10^{13} cm^{-2} and a common maximum energy of 1.5 MeV. [10] © 2004 IEEE.

Next, performances of the SJ-UMOSFET adopting the above p–columns (N= 4) are investigated. Fig. 3-12 shows drain current characteristics (I_d-V_{ds}) at the V_{gs} of 10 V for 4.0-μm cell U-MOSFET and SJ-UMOSFET, which have the V_B of approximately 80 V. By introducing the superjunction structure, the drain current increased drastically, while the V_B is maintained almost constant. This is because the resistivity and the thickness of the n–epi layer could be reduced by 40% and 20%, respectively. The $R_{ON}A$ reduction is over 30% at V_{gs} = 10 V.

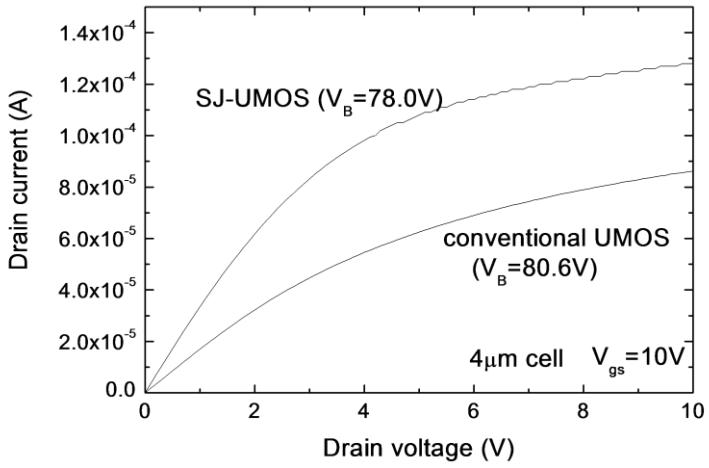
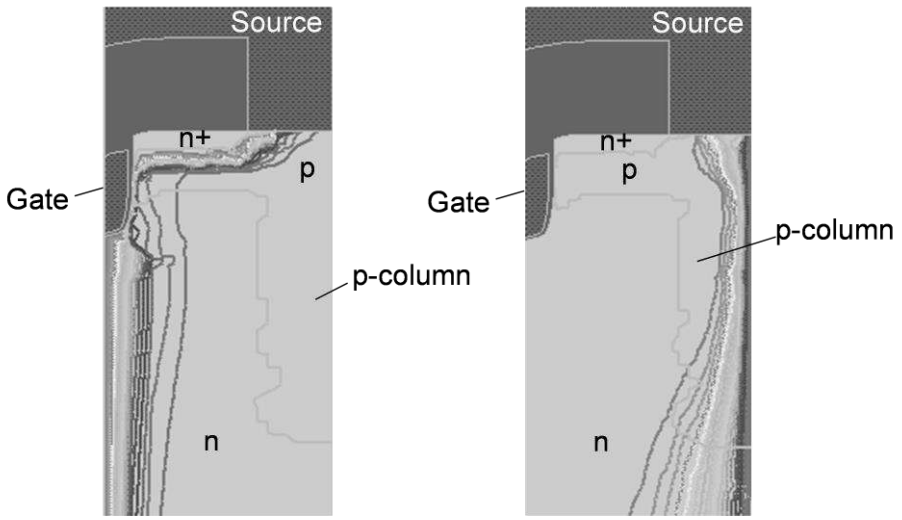


Fig. 3-12. Simulated I_d–V_{ds} characteristics of the SJ-UMOSFET and conventional U-MOSFET are compared for 4-μm cell devices. [10] © 2004 IEEE.

Fig. 3-13 shows avalanche current flow lines at room temperature of the SJ-UMOSFETs for N = 4, in comparison of two different p–column dose conditions. To ensure the high avalanche immunity, the avalanche current through the p–column is preferred, but not vicinity of the trench gate. When the p–column dose is enough high, the preferable current flow is confirmed as shown in Fig. 3-13(b).



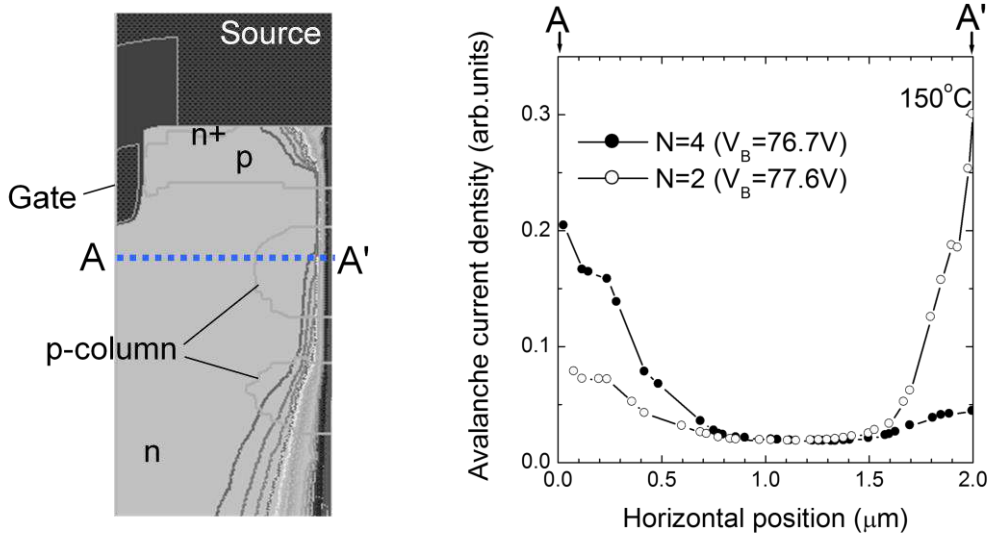
(a) N= 4, p–column: 2.0×10^{12} cm^{-2}, and room temperature.

(b) N= 4, p–column: 2.5×10^{12} cm^{-2}, and room temperature.

Fig. 3-13. Simulated avalanche current flow lines at room temperature of the SJ-UMOSFETs for N= 4, in comparison of two different p–column dose conditions. [10] © 2004 IEEE (modified).

It is better to use a higher dose for the p–column, however, since the avalanche current causes self-heating, the current path should be characterized at a higher temperature. Fig. 3-14(a) shows the avalanche current flow lines at room temperature for N= 2. In this structure, the current flows through the p–column region. This means that gate oxide damage can be avoided when breakdown occurs at room temperature.

Fig. 3-14(b) shows the lateral distribution of the avalanche current that flows at 150°C across the horizontal plane in the middle depth of the p–column. At this temperature, the current flows mainly through the p–column for N = 2, while it flows preferably along the trench gate for N= 4. This difference can be explained by the fact that higher impurity concentration causes higher field modulation at the bottoms of the p–column regions.



(a) N= 2, p–column: 2.5×10^{12} cm^{-2}, and room temperature

(b) 150°C

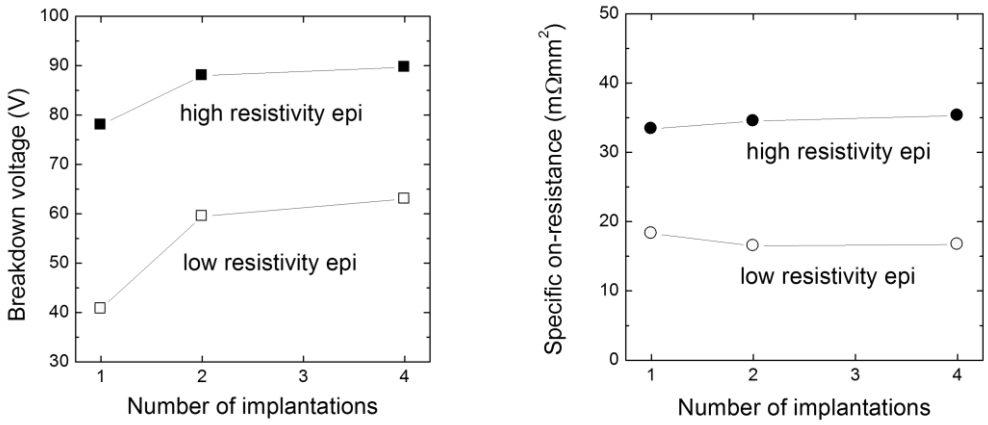
Fig. 3-14. (a) Simulated avalanche current flow lines at room temperature of the SJ-UMOSFET for N= 2. (b) Avalanche current density at 150°C across the horizontal plane in the middle depth of the p–column, in comparison of N=2 and N= 4. [64] © 2005 IEEE (modified).

The simulated results demonstrate that the present device structures are quite promising to achieve ultra-low on-resistance. Further, the multiple implantation technique would be suitable for the SJ-UMOSFET fabrication, because the superjunction structures can be modified flexibly by altering implantation conditions to achieve better device performance and higher reliability.

As shown in Fig. 3-8(b), the SJ-UMOSFET with split p–column structures consists of p–islands separated by small distances in the n–epi layer. The structure is shown to have good avalanche current properties, and it is expected that ultralow $R_{ON}A$ and good dynamic properties can be achieved.

Fig. 3-15 shows the V_B and the $R_{ON}A$ for N = 4, 2, and 1, in comparison of two types of n–epi layers. The V_B dependence on N indicates that the superjunction effect is large as compared with conventional U-MOSFETs without p–column (N = 0), which are 52.4 V and 35.8 V. It is notable that the V_B of N = 2 are as high as those of N = 4 for both types of n–epi layers, while the V_B of N = l is significantly lower than those of the formers. On the other hand, the $R_{ON}A$ does not change depending on N.

In this way, the simulated results demonstrate that the split p–column structure is effective for improving the avalanche current properties, without sacrificing the benefits of the superjunction structure.



(a) (b)

Fig. 3-15. (a) V_B and (b) $R_{ON}A$ of optimized SJ-UMOSFETs for N = 4, 2, and 1, in comparison of two types of n–epi layers. [64] (modified).

3.2.3.2. Process evaluation for superjunction structure

As previous evaluation of the SJ-UMOSFET, a simple SJ-diode consisting of deep p–columns in n–epi layers was fabricated. The p–columns with 3-μm pitch were formed by multiple boron implantations using mask patterns. The maximum implantation energies were set at 1.5 MeV and 2.0 MeV, with $N = 4$ and $N = 5$ injections, respectively. The thickness and impurity concentrations in the n–epi layers were varied to evaluate the charge balance conditions.

Fig. 3-16 shows the cross-sectional scanning capacitance microscopy (SCM) image of the SJ-diodes fabricated by boron implantations up to 2.0 MeV. The p–columns are indicated by the vertically expanding bright regions with depth of 3.0 μm and width of 1.0 μm. Dark lines clearly defining the p/n interfaces suggest that abrupt pn-junctions are formed throughout the SJ-diode process. This shape indicates that the sidewalls of the pn-junction are free from laterally swelling geometries, which should appear after excessive annealing. The ion scattering at the window edges is thought to play a crucial role in forming flat and abrupt pn-junctions, which are favorable characteristics to reduce the $R_{ON}A$.

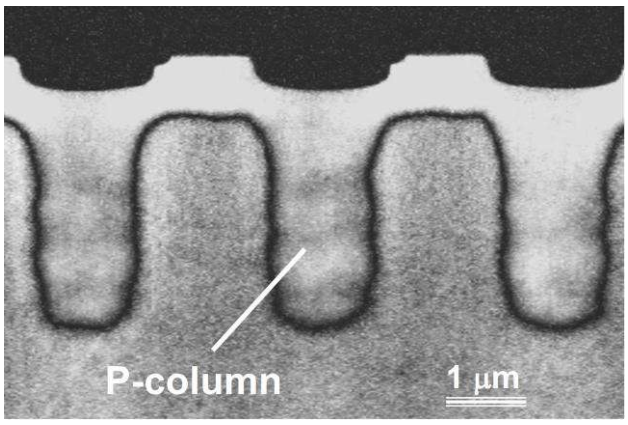


Fig. 3-16. SCM image of SJ-diode with cell pitch of 3.0 μm. [10] © 2004 IEEE.

3.2.3.3. Experimental results of device performance

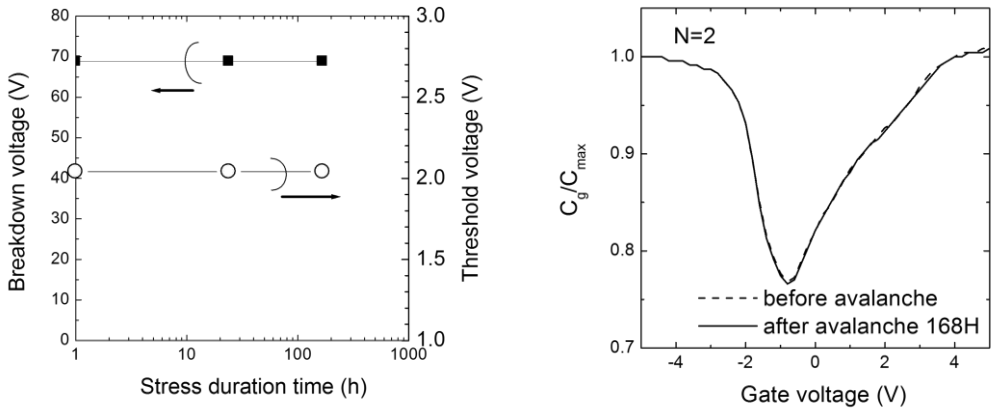
Fabricated 3.0-μm pitch SJ-UMOSFET with split p–column structures using the multiple-ion-implantations method was evaluated. The p–columns were arranged symmetrically in trench gate patterns. The maximum energy of the implantation energy was set at 1.5 MeV and the number of implantations at $N = 2$. In this fabricated SJ-UMOSFET, the V_B was 68.8 V.

A. Repetitive inductive switching properties

To investigate the avalanche robustness of the SJ-UMOSFET, it was examined how the device properties are affected by repetitive avalanche stress, where pulsed avalanche currents are repetitively forced to flow in the device under controlled maximum channel temperatures. The repetitive avalanche test was performed by packaged device. The maximum channel temperature was set at 175°C, and avalanche current at 25 A, by adjusting the pulse width and frequency calculated from the measured thermal resistance values. The inductance load was 10 μH.

Fig. 3-17(a) shows the V_B and the V_{TH} as a function of stress duration time up to 168 hours. In this test, any change in both properties was not observed. To check the avalanche damage more sensitively, capacitance–voltage (C–V) curve shifts of the gate oxide after the avalanche current stress were examined. The C–V measurements at 100 kHz were performed for the devices with a biased gate and with a grounded source and drain. As shown in Fig. 3-17(b), no C–V curve shifts after the 168 hours stress was observed. This means that the avalanche current did not cause any charges in the gate oxide.

These results support that the present SJ-UMOSFET has strong immunity against repetitive inductive switching, because of preferential avalanche current path through the p–columns.



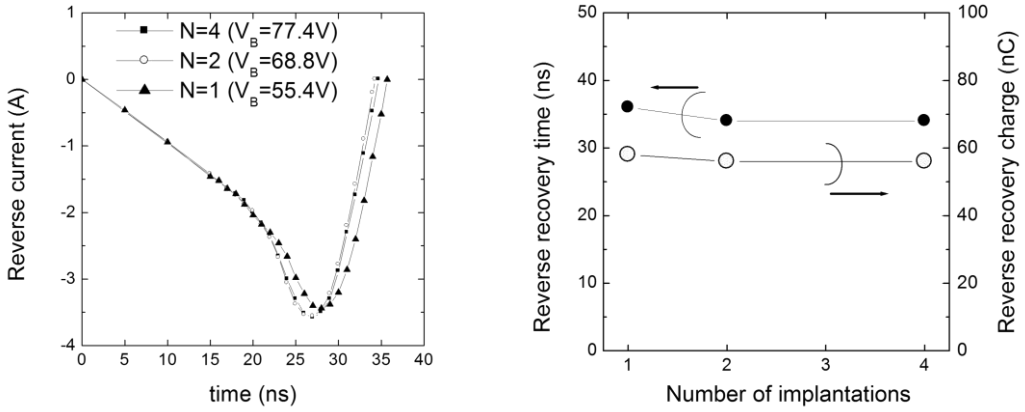
(a) (b)

Fig. 3-17. (a) Time dependence of the V_B and the V_{TH}, after the repetitive avalanche stress. (b) C–V curves before and after the repetitive avalanche stress, for 168 hours at 175°C. [64] © 2005 IEEE (modified).

B. Reverse recovery properties

Modification of the p–column structure would possibly change the body diode properties. To investigate such effects, reverse recovery properties of the body diode for three kinds of SJ-UMOSFETs corresponding to N = 4, 2, and 1 were measured. The V_B of the devices with N = 4, 2, and 1 were 77.4 V, 68.8 V, and 55.4 V, respectively. Fig. 3-18(a) shows the time dependence of the reverse current under the condition of di/dt at 100 A/μs. For all curves, slight current enhancement takes place with onset point at around 20 ns. Since the reverse voltage starts to increase at this onset point, the excess current component is attributed to the depletion charge. The maximum reverse voltage is in the small voltage range (~1.5 V), the relevant change is originated from the depletion region along the pn-junction.

In Fig. 3-18(b), the calculated reverse recovery time (t_{rr}) and reverse recovery charge (Q_{rr}) were compared for N= 4, 2, and 1. No significant difference among the samples was observed. This means that the split p–column structure brings no harmful effects on the reverse recovery properties.



(a) (b)

Fig. 3-18. (a) Time dependence of the reverse current of body diode under the condition of *di/dt* at 100 A/μs, and (b) reverse recovery time and reverse recovery charge of body diode, for SJ-UMOSFETs fabricated with N= 4, 2, and 1 [64] © 2005 IEEE (modified).

C. On-resistance

The tradeoff relationship between the V_B and the $R_{ON}A$ is shown in Fig. 3-19. By optimizing the SJ-UMOSFET design with N = 2, the performance was improved by approximately 25% compared with that with N= 4. The best performance with $R_{ON}A$ of 28.7 mΩ·mm^2 at V_{gs} of 10 V for V_B of 68.0 V for the split p–column structure.

The best performances obtained from the simulation for various epi-layer designs were also plotted in Fig. 3-19. These data strongly suggests that the proposed split p–column structure is quite effective to achieve high performance of 40–80-V-rated LV-MOSFETs.

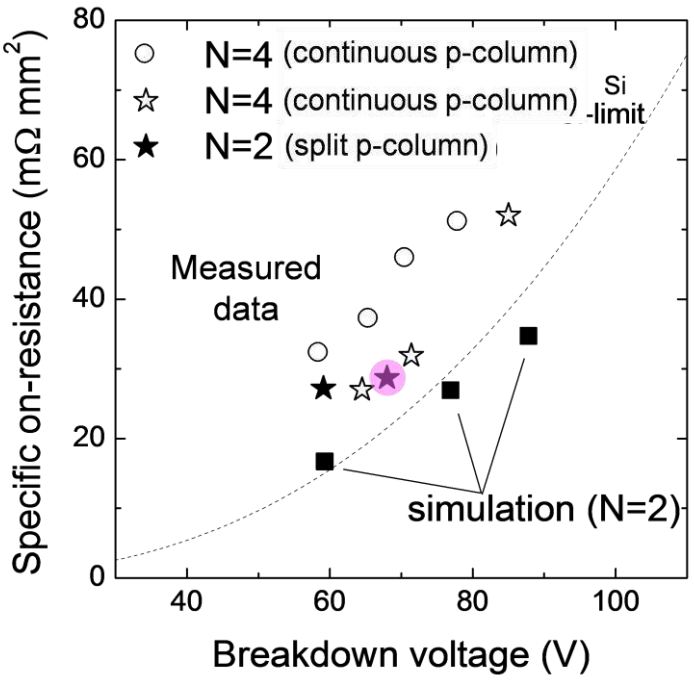


Fig. 3-19. Tradeoff between V_B and $R_{ON}A$ for 3.0-μm pitch SJ-UMOSFETs. The measured best performance shows $R_{ON}A$ = 28.7 mΩ·mm² and V_B = 68.0 V. [64] © 2004 IEEE (modified).

3.2.4. Validation of on-resistance model

Fig. 3-20 shows the $R_{ON}A$ of developed 60-V-class SJ-UMOSFET compared with that of both analytical model (Eqs. (3-11)–(3-22)) and TCAD simulation. The structural parameters, electrical parameters and physical constants are indicated in Table 3-3, Table 3-4 and Table 2-4. In the case of stripe cell that has both continuous channel and continuous p–column in longer direction of trench, the $R_{ON}A$ at V_{gs} = 10 V calculated by the model is 31.7 mΩ·mm², which corresponds to TCAD result of 31.6 mΩ·mm² very well. In this developed SJ-UMOSFET structure, Eq. (3-18) is amended to Eq. (3-23) because current flow at the top of n–column layer is assumed full expansion rather than 45 degrees.

$$R_{D1\_P}\mathrm{A} = \frac{\rho_D W_{Cell}}{W_N - W_{Dep\_N}}\left(T_{SJ} - L_A\right) \tag{3-23}$$

Moreover, actual developed SJ-UMOSFET has the square cell geometry, as shown in Fig. 3-6(a). In the case of square cell, the $R_{ON}A$ at V_{gs} = 10 V calculated by the model is 29.6 mΩ·mm², which corresponds to the experimental result of 28.7 mΩ·mm², with only 3.1% error.

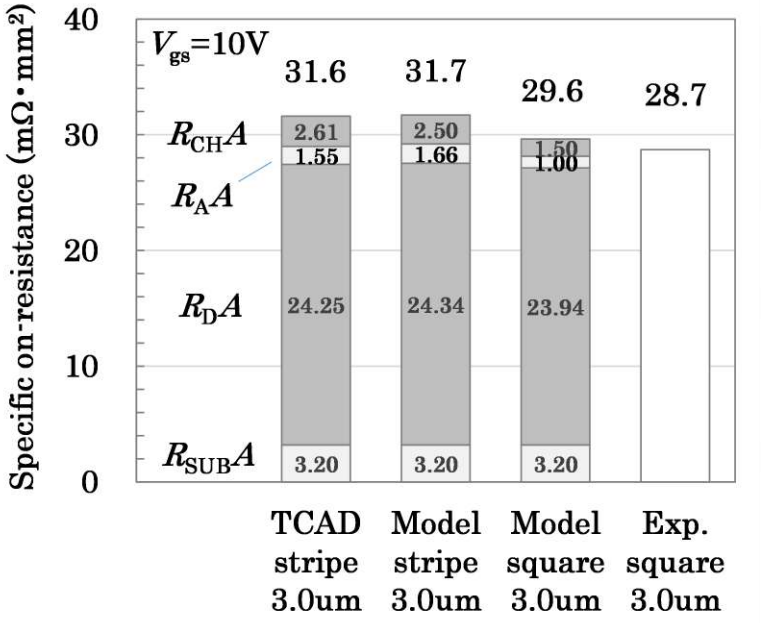


Fig. 3-20. Experimental results of $R_{ON}A$ for developed 60-V-class SJ-UMOSFET compared with that of both analytical model and TCAD simulation. Under the condition of V_{gs} = 10 V.

Table 3-3. Structural parameters of 60-V-class SJ-UMOSFET to calculate $R_{ON}A$.

Symbol	Parameters	Numerics	Unit
W_{Cell}	Cell width	3.00	μm
W_T	Trench width	0.50	μm
W_{Mesa}	Mesa width	2.50	μm
D_T	Trench depth	1.00	μm
L_{CH}	Channel length	0.40	μm
L_A	Accumulation length	0.35	μm
K_A	Coefficient of current spreading in the accumulation region	0.70	
T_{GOX}	Gate oxide thickness	0.05	μm
X_{JS}	n^+–Source junction depth	0.20	μm
X_{JB}	p–Base junction depth	0.60	μm
W_P	p–Column width	1.00	μm
W_N	n–Column width	2.00	μm
T_{SJ}	p–Column layer thickness	1.90	μm
T_{BUF}	n–Buffer thickness	1.50	μm
ρ_D	Resistivity of n–Drift layer	0.50	Ω・cm
N_D	Drift layer concentration	1.04×10^{16}	atoms/cm^3
N_A	p–Column layer concentration	1.60×10^{16}	atoms/cm^3
T_{SUB}	n^+–Substrate thickness	200	μm
ρ_{SUB}	Resistivity of n^+–substrate	0.0016	Ω・cm
N_{SUB}	n^+–Substrate concentration	4.32×10^{19}	atoms/cm^3

Table 3-4. Electrical parameters of 60-V-class SJ-UMOSFET to calculate $R_{ON}A$.

Symbol	Parameters	Numerics	Unit
V_{gs}	Gate–source voltage	10	V
V_{TH}	Threshold voltage	3.05	V
μ_{ni}	Electron mobility of inversion layer	500	cm^2/Vs
μ_{na}	Electron mobility of accumulation layer	550	cm^2/Vs
μ_{n_D}	Electron mobility of n–drift layer	1000	cm^2/Vs
μ_{n_SUB}	Electron mobility of n^+–substrate	76.6	cm^2/Vs
V_{bi}	Built-in potential between p–column and n–column	0.70	V
V_{ON}	On-state voltage	0.10	V

3.3. Field-plate MOSFET (FP-MOSFET) approaching ultimate structure

The FP-MOSFET has the field plate inside the trench and the field plate is connected to the gate or the source electrode. They are distinguished to gate field-plate (GFP) structure and source field-plate (SFP) structure, respectively, as needed. In the off-state, an electric field in the drift region between trenches is reduced by the field-plate effect through a thick oxide. Therefore, despite the higher doping concentration of the drift layer than that in the D-MOSFET, high V_B and low $R_{ON}A$ can be obtained at the same time. Among the LV-MOSFETs' rated-voltage, 60–150 V FP-MOSFETs, which could obtain relatively large effect, were reported in early development stage [8] [50] [49] [51] [17], subsequently the applied devices were expanded to lower rated-voltage [52].

On the other hand, the process technology to realize the device structure is more complex than not only the U-MOSFET but also the SJ-UMOSFET. Thus, a uniform thick oxide which separates the field-plate and the mesa region is applied as standard structure. However, as one of the advanced FP-MOSFET, a slant field-plate structure has been devised and its superior $R_{ON}A$–V_B characteristics were reported as simulation results [65] [66] [67] [68]. In the slant field-plate structure having a gradient thick oxide, the electric field of the mesa region is distributed more uniformly in the vertical direction, and the structure can achieve high MOSFET performance.

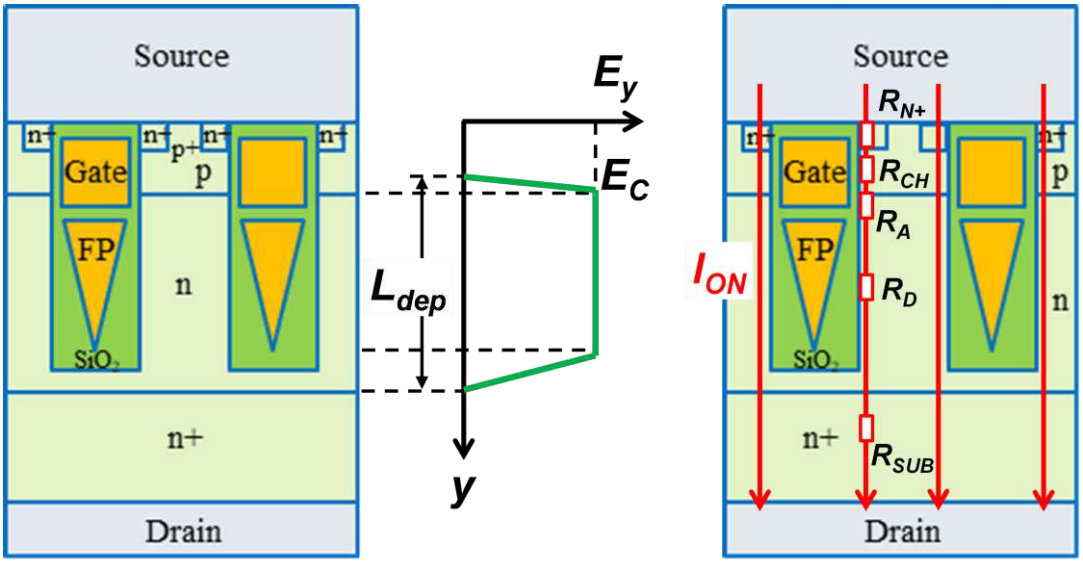
3.3.1. Basic structure and on-resistance ($R_{ON}A$) components of FP-MOSFET

Schematic cross-sectional structure of FP-MOSFET for two unit-cells area is shown in Fig. 3-21(a) shows a distribution of electric field E_y of drift layer in vertical direction y, when reverse bias applies to drain. In an ideal FP-MOSFET, the E_y is distributed like a trapezoid and a critical electric field E_C is nearly uniform, which are the almost same as those of the SJ-UMOSFET.

Since V_B of two-dimensional is determined by the area of this electric field, the V_B of FP-MOSFET is approximated as

$$V_B \approx \int_0^{L_{dep}} E_C dy. \tag{3-24}$$

Here L_{dep} is the depletion layer length in the depth y direction. In assumption, if the depletion layer length in the p–base region is negligible, the V_B of FP-MOSFET is approximated as



(a) (b)

Fig. 3-21. Schematic cross-sectional structures of FP-MOSFET, which shows two unit-cells area. (a) Electric field distribution in vertical direction of off-state. (b) On-state current paths and components of on-resistance.

$$V_B \approx E_C(L_D - T_{BUF}) + \frac{1}{2}E_C T_{BUF}, \tag{3-25}$$

where L_D is the n–drift layer length and T_{BUF} is the buffer layer thickness under the trench, which shares a part of the V_B. The V_B of FP-MOSFET is independent from N_D in same manner to the SJ-MOSFET. The V_B and the R_{DA} has a nearly linear relationship that is described as $R_{DA} \propto V_B^{1.1}$ in [60].

Fig. 3-21(b) shows on-state current paths and on-resistance components of the FP-MOSFET. The R_{N+A} is negligible as like that of the U-MOSFET or the SJ-UMOSFET. The R_{ONA} of FP-MOSFET ($R_{ON}^{FPMOS}A$) can be approximated by using main components,

$$R_{ON}{}^{FPMOS}\mathrm{A} \approx R_{CH}A + R_A A + R_D A + R_{SUB}A. \tag{3-26}$$

Fundamentally, the FP-MOSFETs are classified to two different types: gate field-plate (GFP) structure [8] [50] [49] [51] [17], as shown in Fig. 3-22(a), and source field-plate (SFP) structure [52] [69] [70] [71], as shown in Fig. 3-22(b). In the GFP-MOSFET, the field plate is being continuous to the gate electrode as one body, so that the GFP-MOSFET has lower R_{ONA} due to an accumulation channel effect along the trench

sidewall in the mesa region. However, higher gate–drain capacitance (C_{gd}) is one of the disadvantage. On the other hand, in the SFP-MOSFET, the field plate is separated from the gate electrode and connected to the source electrode in the device termination region. Thus, the gate electrode inside the trench is shielded from the drain region by the grounded field-plate. Therefore, the SFP-MOSFET has very small C_{gd}, however, the $R_{ON}A$ is slightly higher than that of the GFP-MOSFET.

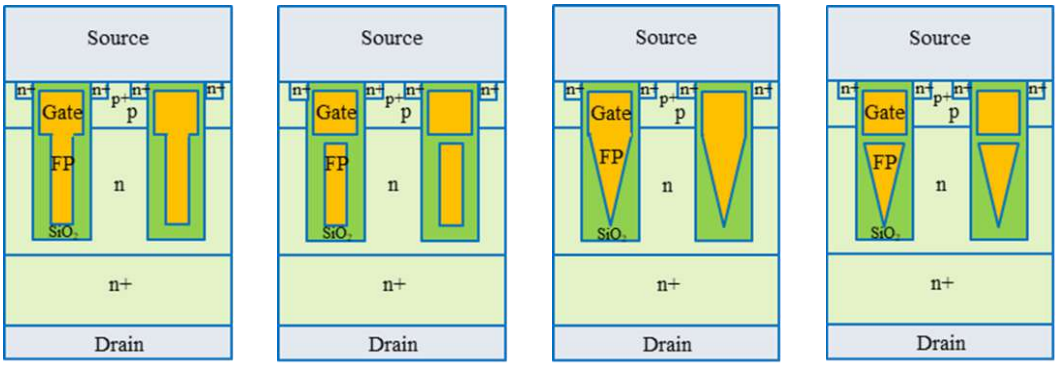


Fig. 3-22. Classification of FP-MOSFETs. (a) GFP-MOSFET with flat field-plate, (b) SFP-MOSFET with flat field-plate, (c) GFP-MOSFET with slant field-plate, and (d) SFP-MOSFET with slant field-plate.

Fig. 3-23 shows structural parameters of SFP-MOSFET. Each of the resistances included in Eq. (3-26) is expressed by analytical model as below.

$$R_{CH}A = \frac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}(V_{gs} - V_{TH})} \tag{3-27}$$

$$R_A A = \frac{L_A W_{Cell}}{2\mu_{na} C_{GOX} V_{gs}} \tag{3-28}$$

$$R_{SUB}\mathrm{A} = \rho_{SUB} T_{SUB} \tag{3-29}$$

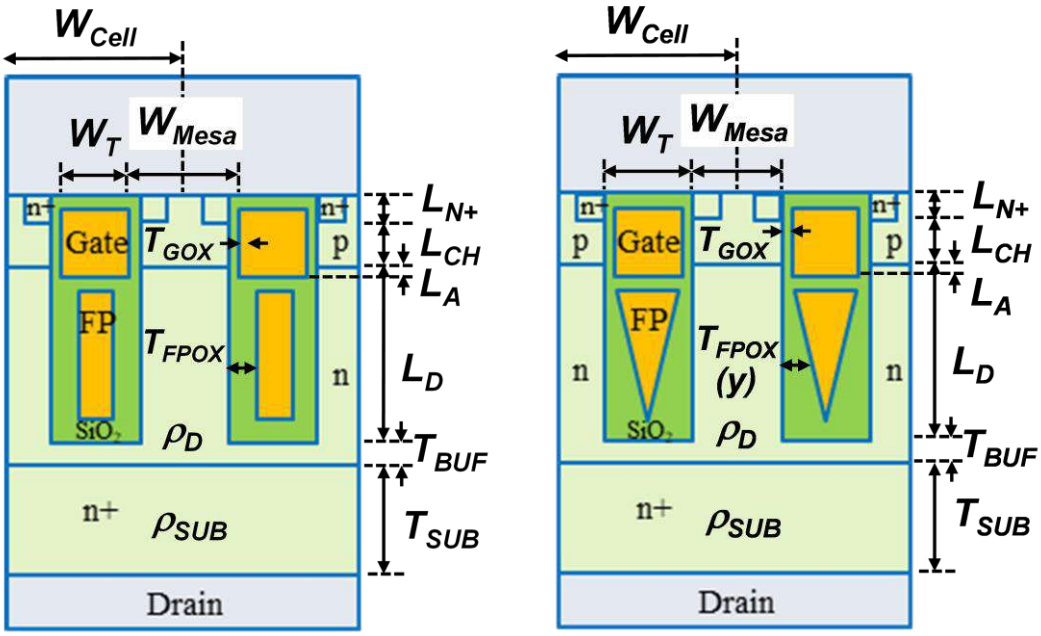


Fig. 3-23. Structural parameters of SFP-MOSFET (a) with flat field-plate and (b) with slant field-plate.

Here, W_{Cell} is the unit cell width and other same symbols are the same as those of subsection 2.2.1, i.e., L_{CH} is the channel length, L_A is the accumulation length, ρ_{SUB} is the resistivity of n^+–substrate, T_{SUB} is the thickness of the n^+–substrate, μ_{ni} is the electron mobility of inversion layer, μ_{na} is the electron mobility of accumulation layer, C_{GOX} is the gate oxide capacitance, V_{gs} is the gate voltage, and V_{TH} is the threshold voltage.

In addition, R_DA in Eq. (3-26) consists of different components depending on the field-plate structure, as shown in Fig. 3-24(a)–(c), R_DA is expressed by analytical model as below.

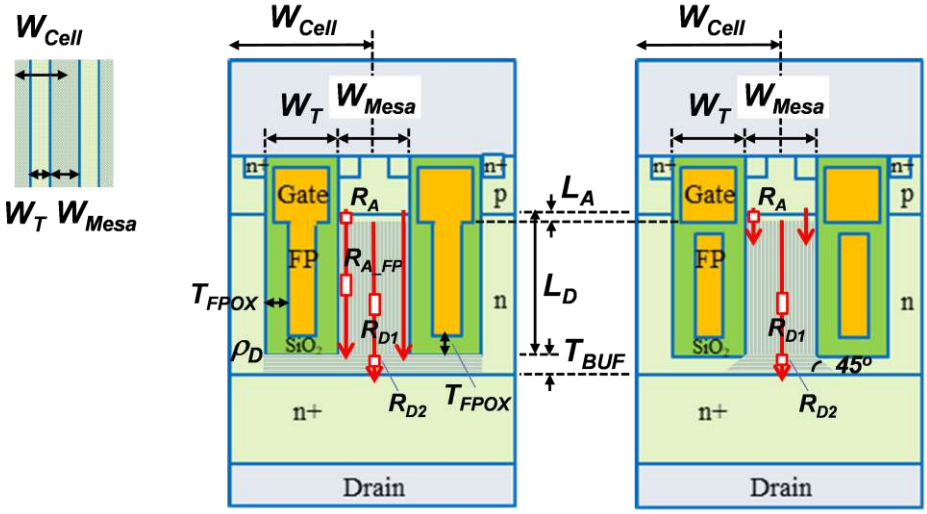
$$R_DA = \begin{cases} \dfrac{R_{D1}A \cdot R_{A\_FP}A}{R_{D1}A + R_{A\_FP}A} + R_{D2}A, & \text{in GFP} - \text{MOSFET} \\ R_{D1}A + R_{D2}A, & \text{in SFP} - \text{MOSFET} \end{cases} \tag{3-30}$$

$$R_{A\_FP}\text{A} = \frac{W_{Cell}}{2} \cdot \frac{(L_D - L_A - T_{FPOX}) + K_A\left(T_{FPOX} + \dfrac{W_T}{2}\right)}{\mu_{na} C_{FPOX} V_{gs}} \tag{3-31}$$

$$R_{D1}\mathrm{A} = \frac{W_{Cell}}{W_{Mesa}}\rho_D(L_D - L_A) \tag{3-32}$$

$$R_{D2}A = \begin{cases} \rho_D T_{BUF}, & \text{in GFP} - \text{MOSFET} \\ \dfrac{W_{Cell}}{2}\rho_D \ln\dfrac{W_{Cell}}{W_{Mesa}} + \rho_D\left(T_{BUF} - \dfrac{W_T}{2}\right), T_{BUF} \geq \dfrac{W_T}{2}, & \text{in SFP} - \text{MOSFET} \\ \dfrac{W_{Cell}}{2}\rho_D \ln\dfrac{W_{Mesa} + T_{BUF}}{W_{Mesa}}, 0 < T_{BUF} < \dfrac{W_T}{2}, & \text{in SFP} - \text{MOSFET} \end{cases} \tag{3-33}$$

Here, $R_{D1}A$ is the drift layer resistances in the mesa region, $R_{D2}A$ is the drift layer resistances in the buffer layer, and $R_{A\_FP}A$ are the accumulation resistance along the field plate. It is noted that the accumulation layer of the GFP-MOSFET is divided into three portions: along the gate oxide, along the field plate of the mesa region, and along the field plate at bottom corner of the trench. K_A is a coefficient of considering current spreading from the accumulation region to the drift region [25] [26]. In Eq. (3-31), the total accumulation length of the unit cell is given by $2T_{FPOX} + W_T$. K_A is assumed to be around 0.6. In addition, ρ_D is the resistivity of n–drift layer and C_{FPOX} is the field-plate oxide capacitance. C_{FPOX} is calculated by using T_{FPOX}, which is the thickness of the field-plate oxide, and given by



(a) (b) (c)

Fig. 3-24. (a) Top view of FP-MOSFET for stripe cell layout. Schematic cross-sectional structure, which shows components of the accumulation layer and n–drift layer resistance (R_A, R_{A_FP}, R_{D1} and R_{D2}), for (b) GFP-MOSFET and (c) SFP-MOSFET with flat field-plate. Current flow spreading along the field plate in the mesa region and the buffer layer is showing.

$$C_{FPOX} = \frac{\varepsilon_{OX}\varepsilon_0}{T_{FPOX}}. \tag{3-34}$$

In the GFP-MOSFET, the first term of Eq. (3-30) is parallel resistance of $R_{D1}A$ and $R_{A\_FP}A$, thus the R_DA can be reduced by the accumulation effect. Moreover, as the $R_{D2}A$ region, the current flows in whole buffer layer because the accumulation layer of the trench bottom helps it, as shown in Fig. 3-24(b). On the other hand, in the SFP-MOSFET, the R_DA is simply expressed as series resistance of $R_{D1}A$ and $R_{D2}A$ in Eq. (3-30). However, in the $R_{D2}A$ region, the current flow is spreading in 45 degrees from the bottom of the mesa region, as shown in Fig. 3-24(c). Therefore, the R_DA of the SFP-MOSFET shows slightly disadvantage compared with that of the GFP-MOSFET.

As another classification of the FP-MOSFETs, there are two different field-plate shapes: flat field-plate structure described the above, as shown in Fig. 3-22(a)–(b), and slant field-plate structure [65] [66] [67] [68] [72], as shown in Fig. 3-22(c)–(d). In the slant field-plate structure, thick oxide between the mesa region and the field plate has a slope and the thickness increases gradually toward the trench bottom. The ideal FP-MOSFET, which has nearly uniform electric field distribution in the mesa region as shown in Fig. 3-21, is achieved by the slant field-plate structure rather than the flat field-plate structure [72].

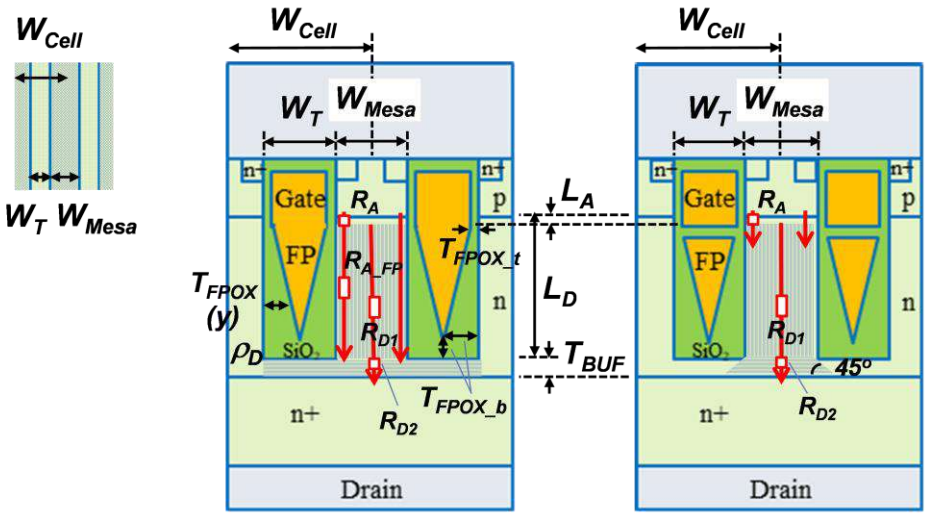
In the slant field-plate structure, the current flow spreading in the accumulation layer and the n–drift layer is the same as that of the flat field-plate structure, as shown in Fig. 3-25(a)–(c). However, in the case of the slant GFP-MOSFET, the accumulation effect along the field plate varies by the field-plate depth. Therefore, the first term in Eq. (3-31) is expressed as

$$R_{A\_FP(1)}\mathrm{A} = \frac{W_{Cell}}{2} \cdot \frac{1}{\mu_{na} V_{gs}} \cdot \int_0^{L_D - L_A - T_{FPOX\_b}} \frac{1}{C_{FPOX}(y)}\, dy. \tag{3-35}$$

Here T_{FPOX_b} is thickness of the field-plate oxide at bottom position. The field-plate oxide capacitance depending the depth $C_{FPOX}(y)$ is expressed by using $T_{FPOX}(y)$, which is thickness of the field-plate oxide depending the depth.

$$C_{FPOX}(\mathrm{y}) = \frac{\varepsilon_{OX}\varepsilon_0}{T_{FPOX}(y)}. \tag{3-36}$$

The $T_{FPOX}(y)$ is given by



(a) (b) (c)

Fig. 3-25. (a) Top view of FP-MOSFET for stripe cell layout. Schematic cross-sectional structure, which shows components of the accumulation layer and n–drift layer resistance (R_A, R_{A_FP}, R_{D1} and R_{D2}), for (b) GFP-MOSFET and (c) SFP-MOSFET with slant field-plate. Current flow spreading along the field plate in the mesa region and the buffer layer is showing.

$$T_{FPOX}(\mathrm{y}) = \mathrm{y} \cdot \frac{T_{FPOX\_b} - T_{FPOX\_t}}{L_D - L_A} + T_{FPOX\_t}. \tag{3-37}$$

where T_{FPOX_t} is thickness of the field-plate oxide at top position. By substituting Eqs. (3-36)–(3-37) into Eq. (3-35), the following is obtained.

$$R_{A\_FP(1)}\mathrm{A} = \frac{W_{Cell}}{2\mu_{na}\varepsilon_{OX}\varepsilon_0 V_{gs}} \cdot \frac{\left(L_D - L_A - T_{FPOX\_b}\right)\left(T_{FPOX\_b} + T_{FPOX\_t}\right)}{2} \tag{3-38}$$

Therefore, in the slant GFP-MOSFET, $R_{A\_FP}A$ in Eq. (3-31) has to be amended model as below.

$$R_{A\_FP}\mathrm{A} = \frac{W_{Cell}}{2\mu_{na}\varepsilon_{OX}\varepsilon_0 V_{gs}} \left[\frac{\left(L_D - L_A - T_{FPOX\_b}\right)\left(T_{FPOX\_b} + T_{FPOX\_t}\right)}{2} + K_A \left(T_{FPOX\_b} + \frac{W_T}{2}\right) T_{FPOX\_b} \right] \tag{3-39}$$

To improve the $R_{ON}{}^{FPMOS}A$ with necessary V_B maintained, all the components of $R_{ON}{}^{FPMOS}A$ have to be reduced by individual appropriate techniques.

3.3.2. List of on-resistance model

Table 3-5. List of $R_{ON}A$ model equations for GFP-MOSFET and SFP-MOSFET with flat field-plate (stripe cell design).

Flat GFP-MOSFET, stripe	Flat SFP-MOSFET, stripe
$R_{CH}\mathrm{A} = \dfrac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}$	$R_{CH}\mathrm{A} = \dfrac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}$
$R_{A}\mathrm{A} = \dfrac{L_{A}W_{Cell}}{2\mu_{na}C_{GOX}V_{gs}}$	$R_{A}\mathrm{A} = \dfrac{L_{A}W_{Cell}}{2\mu_{na}C_{GOX}V_{gs}}$
$R_{D}\mathrm{A} = \dfrac{R_{D1}A \cdot R_{A\_FP}A}{R_{D1}A + R_{A\_FP}A} + R_{D2}A$	$R_{D}\mathrm{A} = R_{D1}A + R_{D2}A$
$R_{D1\_P}\mathrm{A} = \dfrac{W_{Cell}}{W_{Mesa}}\rho_D(L_D - L_A)$	$R_{D1}\mathrm{A} = \dfrac{W_{Cell}}{W_{Mesa}}\rho_D(L_D - L_A)$
$R_{D2\_P}\mathrm{A} = \rho_D T_{BUF}$	$R_{D2}\mathrm{A} = \begin{cases} \dfrac{W_{Cell}}{2}\rho_D \ln\dfrac{W_{Cell}}{W_{Mesa}} + \rho_D\left(T_{BUF} - \dfrac{W_T}{2}\right) \\ \qquad , T_{BUF} \geq \dfrac{W_T}{2} \\ \dfrac{W_{Cell}}{2}\rho_D \ln\dfrac{W_{Mesa}+T_{BUF}}{W_{Mesa}} \\ \qquad , 0 < T_{BUF} < \dfrac{W_T}{2} \end{cases}$
$R_{A\_FP}\mathrm{A} = \dfrac{W_{Cell}}{2} \cdot \dfrac{(L_D - L_A - T_{FPOX}) + K_A\left(T_{FPOX} + \dfrac{W_T}{2}\right)}{\mu_{na}C_{FPOX}V_{gs}}$	
$R_{SUB}\mathrm{A} = \rho_{SUB}T_{SUB}$	$R_{SUB}\mathrm{A} = \rho_{SUB}T_{SUB}$

Table 3-6. List of $R_{ON}A$ model equations for GFP-MOSFET and SFP-MOSFET with slant field-plate (stripe cell design).

Slant GFP-MOSFET, stripe	Slant SFP-MOSFET, stripe
$R_{CH}\mathrm{A} = \dfrac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}$	$R_{CH}\mathrm{A} = \dfrac{L_{CH}W_{Cell}}{2\mu_{ni}C_{GOX}(V_{gs}-V_{TH})}$
$R_{A}\mathrm{A} = \dfrac{L_{A}W_{Cell}}{2\mu_{na}C_{GOX}V_{gs}}$	$R_{A}\mathrm{A} = \dfrac{L_{A}W_{Cell}}{2\mu_{na}C_{GOX}V_{gs}}$
$R_{D}\mathrm{A} = \dfrac{R_{D1}A \cdot R_{A\_FP}A}{R_{D1}A + R_{A\_FP}A} + R_{D2}A$	$R_{D}\mathrm{A} = R_{D1}A + R_{D2}A$
$R_{D1\_P}\mathrm{A} = \dfrac{W_{Cell}}{W_{Mesa}}\rho_D(L_D - L_A)$	$R_{D1}\mathrm{A} = \dfrac{W_{Cell}}{W_{Mesa}}\rho_D(L_D - L_A)$
$R_{D2\_P}\mathrm{A} = \rho_D T_{BUF}$	$R_{D2}\mathrm{A} = \begin{cases} \dfrac{W_{Cell}}{2}\rho_D \ln\dfrac{W_{Cell}}{W_{Mesa}} + \rho_D\left(T_{BUF} - \dfrac{W_T}{2}\right) \\ \qquad , T_{BUF} \geq \dfrac{W_T}{2} \\ \dfrac{W_{Cell}}{2}\rho_D \ln\dfrac{W_{Mesa}+T_{BUF}}{W_{Mesa}} \\ \qquad , T_{BUF} < \dfrac{W_T}{2} \end{cases}$
$R_{A\_FP}\mathrm{A} = \dfrac{W_{Cell}}{2\mu_{na}\varepsilon_{OX}\varepsilon_0 V_{gs}}\left[\dfrac{(L_D - L_A - T_{FPOX\_b})(T_{FPOX\_b}+T_{FPOX\_t})}{2} + K_A\left(T_{FPOX\_b}+\dfrac{W_T}{2}\right)T_{FPOX\_b}\right]$	
$R_{SUB}\mathrm{A} = \rho_{SUB}T_{SUB}$	$R_{SUB}\mathrm{A} = \rho_{SUB}T_{SUB}$

3.3.3. 100-V multiple-stepped-oxide GFP-MOSFET [3]

Applying the FP-MOSFET is expanding to improve the performances in wide range LV-MOSFETs products this decade. As described above, the slant FP-MOSFET which has an ideal field-plate structure has been devised, however, the real device and the electrical characteristics were not reported so far, because of difficulty of the fabrication process. As one of the approach to realize the slant FP-MOSFET, a multiple stepped oxide FP-MOSFET (MSO-FP-MOSFET), which is extremely close to ideal gradient oxide structure, is proposed [72] [73].

In the following, firstly, 100-V-class device structure design is described. Then, optimization of each design parameter by TCAD simulation is discussed. Moreover, realizable fabrication process flow and experimental results of the device are described.

3.3.3.1. Unit-cell structure design

Fig. 3-26(a)–(c) show schematic cross-sectional structures of conventional FP-MOSFET with uniform thick oxide, ideal slant FP-MOSFET with gradient oxide, and proposed MSO-FP-MOSFET. The MSO-FP-MOSFET structure has multiple small stepped oxide film and stepped single domain polycrystalline-silicon field-plate in the trench (Fig. 3-26(c)).

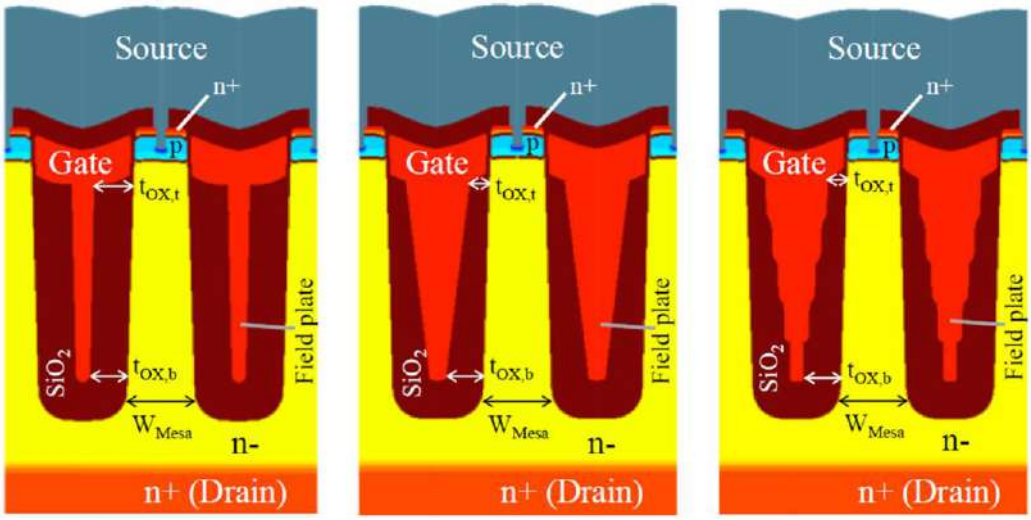
The basic design parameter to achieve V_B of over 100 V is described below. In an ideal FP-MOSFET, the electric field distribution of the mesa region is expected to be uniform in vertical direction in order to maximize the V_B, as shown in Fig. 3-21(a). However, it is difficult to realize completely uniform electric field distribution because a peak of the electric field appears at pn-junction or trench bottom region. Therefore, the V_B in Eq. (3-24) is expressed as

$$V_B = E_C L_D \beta, \tag{3-40}$$

where β is a field coefficient ($0 < \beta < 1$) [66]. The E_C is gradually varied by the necessary V_B, and it becomes higher in lower voltage [11].

$$E_C = 8.2 \times 10^5 \cdot {V_B}^{-0.2}\ (V/cm) \tag{3-41}$$

[3] Subsection 3.3.3 is reconstruction of [72] chapter II–IV, © 2015 IEEE, and [73] chapter 2–5. A part of description is modified and comprehensive explanations are additionally provided. Eqs. (2)–(4) of [72] and Eqs. (3)–(5) of [73] are modified to take account of the mesa region against both sides' field-plates.



(a) (b) (c)

Fig. 3-26. Schematic cross-sectional structures of (a) conventional FP-MOSFET with uniform thick oxide, (b) ideal slant FP-MOSFET with gradient oxide, and (c) proposed multiple-stepped-oxide (MSO) FP-MOSFET. [72] © 2015 IEEE (modified), [73].

The E_C is estimated at 3.20×10^5 V/cm to obtain 110 V, which is added 10% margin to the rated-voltage. When β is assumed to 0.75, necessary L_D is calculated as

$$L_D = \frac{V_B}{E_C \beta} = 4.58 \times 10^{-4}\ (cm) = 4.58\ (\mu m). \tag{3-42}$$

An optimum charge density Q_{Opt} in the mesa region against both sides' field-plates is lead from Poisson's equation [11] [59] [72] [74]. Applying the above E_C, the Q_{Opt} is given by

$$Q_{Opt} = \frac{2E_C \varepsilon_{Si} \varepsilon_0}{q} = 4.15 \times 10^{12}\ (atoms/cm^2). \tag{3-43}$$

Then, when the W_{Mesa} is assumed to 1.2 μm, the N_D is calculated as

$$N_D = \frac{Q_{Opt}}{W_{Mesa}} = \frac{4.15 \times 10^{12}}{1.2 \times 10^{-4}} = 3.46 \times 10^{16}\ (atoms/cm^3). \tag{3-44}$$

As basic design of the MSO-FP-MOSFET, the trench depth is determined to 5.5 μm which is added a fabrication process margin to the calculated L_D (4.58 μm), whereas the cell pitch is determined to 3.0 μm in consideration of the W_{Mesa} and necessary field-plate oxide thickness inside the trench.

3.3.3.2. Validation and optimization of design parameters by TCAD simulation

A. Validation of electric potential and electric field distribution

Behavior of the field-plate effect for both conventional FP-MOSFET and MSO-FP-MOSFET is compared by TCAD simulation. In both MOSFETs, the design parameters, as shown in Fig. 3-23 and Fig. 3-25, are basically same. The field-plate oxide thickness at top position (T_{FPOX_t}) and at bottom position (T_{FPOX_b}) are considered as design parameter optimization. In Fig. 3-26, it is noted that the symbols T_{FPOX_t} and T_{FPOX_b} are expressed as $t_{OX,t}$ and $t_{OX,b}$.

When a high reverse bias is applied to drain–source, a depletion layer expands vertically in the mesa region. Fig. 3-27(a)–(i) show two-dimensional (2-D) potential contours and one-dimensional (1-D) electric field distributions at the V_B under the condition of three different N_D, in both conventional FP-MOSFET and MSO-FP-MOSFET.

For low N_D condition (1.0×10^{16} /cm^3), in both structures, the potential lines are dense at bottom of the trench and sparse at upper region of the mesa (Fig. 3-27(a)–(c)). Thus, the field-plate effect is not enough for the mesa region and the V_B is restricted by the punch-through phenomenon.

For medium N_D condition (2.0×10^{16} /cm^3), the potential lines are distributed more uniformly compared with the low N_D case, therefore the V_B increases in both structures (Fig. 3-27(d)–(f)).

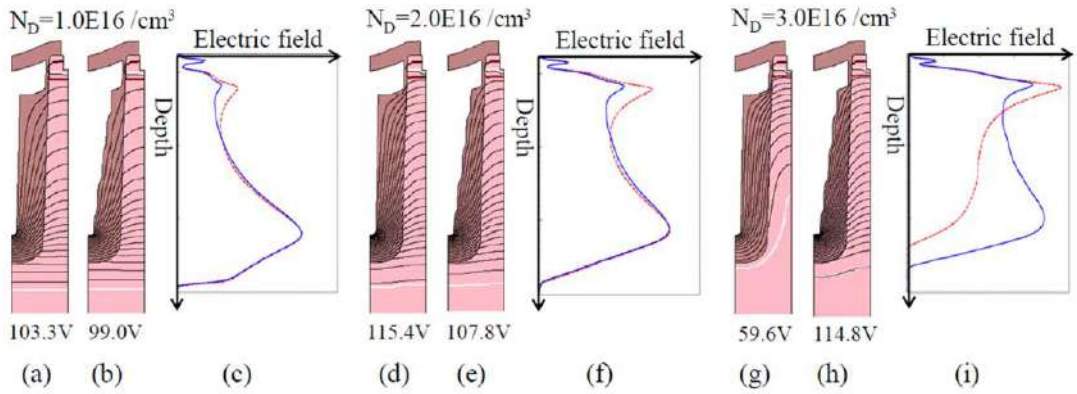


Fig. 3-27. 2-D potential contours at 5-V intervals and 1-D vertical electric field distributions along the trench sidewall. N_D dependence of the potential: (a), (d), and (g) for conventional FP-MOSFETs; and (b), (e), and (h) for MSO-FP-MOSFETs. (c), (f), and (i): N_D dependence of the electric field for conventional FP-MOSFETs (red dashed lines) and MSO-FP-MOSFETs (blue solid lines). [72] © 2015 IEEE, [73].

For high N_D condition (3.0×10^{16} /cm^3), the V_B decreases in the conventional structure because the depletion layer no longer expands enough (Fig. 3-27(g)–(i)). On the other hand, in the MSO-FP-MOSFET, the two peaks of the electric field are nearly equal, and fairly uniform electric field distribution in the vertical direction can be seen. This effect is explained below. The potential lines in the stepped oxide region are distribute laterally with relatively uniform and high density from the bottom to the top, compared with the conventional thick oxide case. Therefore, the potential lines in the mesa region also distribute vertically with approximately equal intervals. In this validated condition, the V_B of 114.8 V can be achieved at 1.5 times higher N_D than that of the conventional FP-MOSFET.

B. Optimization of design parameters

In the FP-MOSFETs shown in Fig. 3-26, the field-plate oxide slope K is defined by

$$K = \frac{L_{FP}}{T_{FPOX\_b} + \frac{L_{FP}}{\tan\alpha} - T_{FPOX\_t}}, \tag{3-45}$$

where L_{FP} is the poly-Silicon field-plate length and α is the trench angle. Regarding significant design parameters (N_D, T_{FPOX_t}, T_{FPOX_b}, and K) which make the V_B change, simulation results are described below.

Fig. 3-28 shows the T_{FPOX_b} ($t_{OX,b}$) dependence of the V_B for various N_D, which is ranged from 1.0×10^{16} to 3.0×10^{16} /cm^3, for the conventional FP-MOSFETs. A basic dependence is seen that the thicker T_{FPOX_b} ($t_{OX,b}$) can rise the V_B. On the other hand, when the N_D increases, a peak V_B decreases.

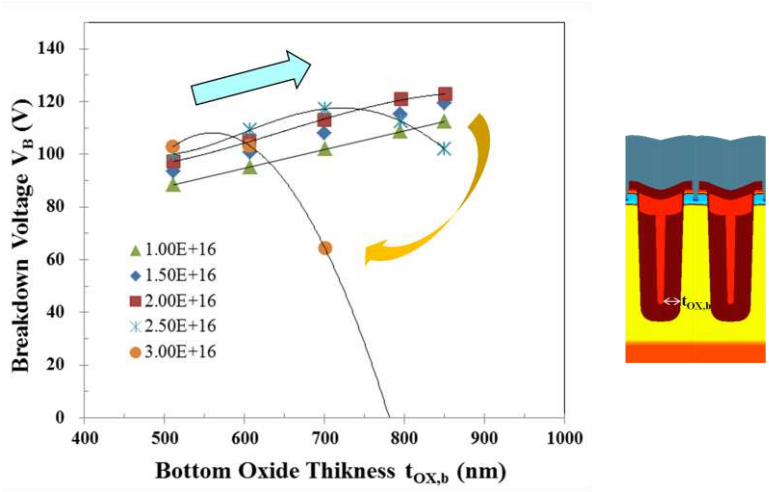


Fig. 3-28. Simulated T_{FPOX_b} ($t_{OX,b}$) dependence of V_B for various N_D in the case of conventional FP-MOSFETs. [73] (modified).

Then, in the MSO-FP-MOSFETs that the T_{FPOX_b} ($t_{OX,b}$) is fixed to 700 nm, the T_{FPOX_t} ($t_{OX,t}$) dependence corresponding to varying K (from 5.5 to 15.5) is simulated. In the simulated conventional FP-MOSFET, K is calculated as 50. As shown in Fig. 3-29, depending on the K, the N_D which obtains the maximum V_B is varied. When the K is smaller, the peak V_B moves to higher N_D side. However, at the same time, the peak V_B decreases in smaller K. Moreover, when the N_D exceeds the peak V_B, the V_B decreases steeply in larger K.

Thus, by adopting the small K, the field-plate effect to reduce the electric field in the mesa region can be achieved, even in the case of the high N_D. It can be seen also in Fig. 3-30. In addition, it is possible that the V_B margin expands to the higher N_D side because the E_C becomes gradually high in the higher N_D [60].

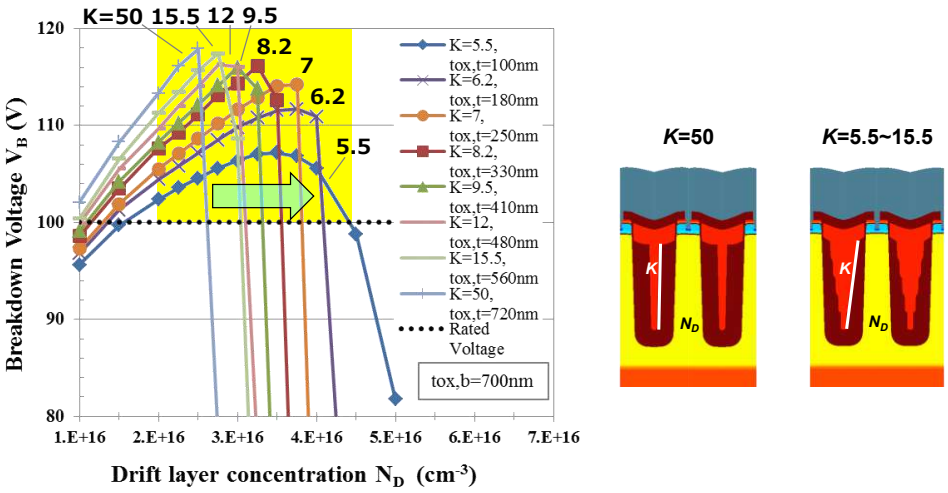


Fig. 3-29. Simulated N_D dependence of V_B for MSO-FP-MOSFETs (K = 5.5–15.5) and conventional FP-MOSFET (K = 50). [73] (modified).

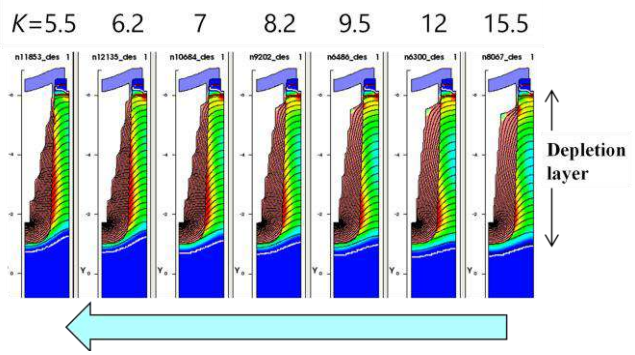


Fig. 3-30. 2-D simulation results for MSO-FP-MOSFETs (K = 5.5–15.5). Depletion layer (white lines), potential contours at 5-V intervals (black lines), and electric field distributions (color) are shown in each half-cell structure.

The $R_{ON}A$ which is dominant for the drift layer resistance decreases corresponding to the N_D increase, as shown in Fig. 3-31. In addition, thinner T_{FPOX_t} ($t_{OX,t}$) has an advantage to reduce $R_{ON}A$ because of an increase of the accumulation effect, in particular along the upper side of the trench.

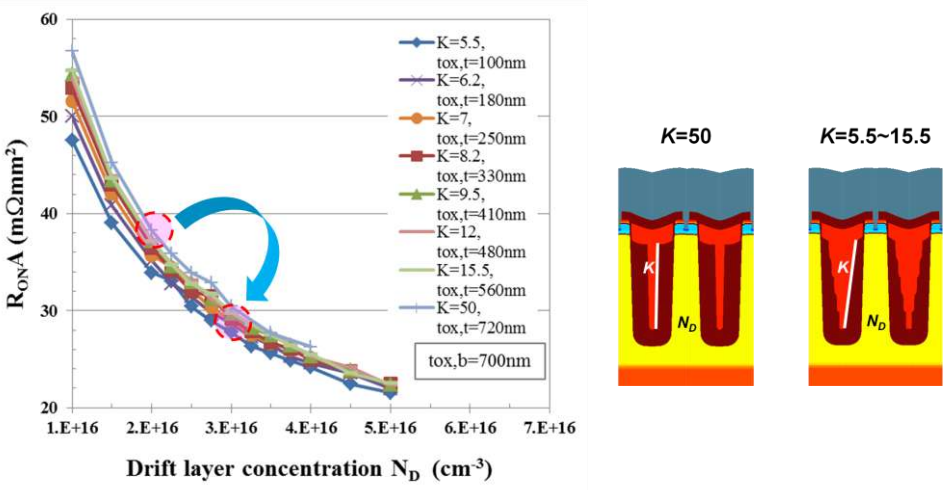


Fig. 3-31. Simulated N_D dependence of $R_{ON}A$ for MSO-FP-MOSFETs (K = 5.5–15.5) and conventional FP-MOSFET (K = 50). [73] (modified).

Based on approximately same V_B margin to the rated-voltage (100 V), both conventional FP-MOSFET and MSO-FP-MSFET has to be compared from the simulation results. In the conventional FP-MOSFET, the V_B is 113.3 V under the conditions of K = 50 and N_D = 2.0×10^{16} /cm^3, and the $R_{ON}A$ becomes 38.2 mΩ·mm^2. In the MSO-FP-MOSFET, the V_B is 111.7 V under the conditions of K = 7 and N_D = 3.0×10^{16} /cm^3, and ultralow $R_{ON}A$ of 29.1 mΩ·mm^2 can be achieved. Here, $R_{ON}A$ is including 1.0 mΩ·mm^2 substrate resistance.

The simulated $R_{ON}A$ of the MSO-FP-MOSFET (29.1 mΩ·mm^2) indicates 25% reduction compared to that of the conventional FP-MOSFET (38.2 mΩ·mm^2) in the same V_B range.

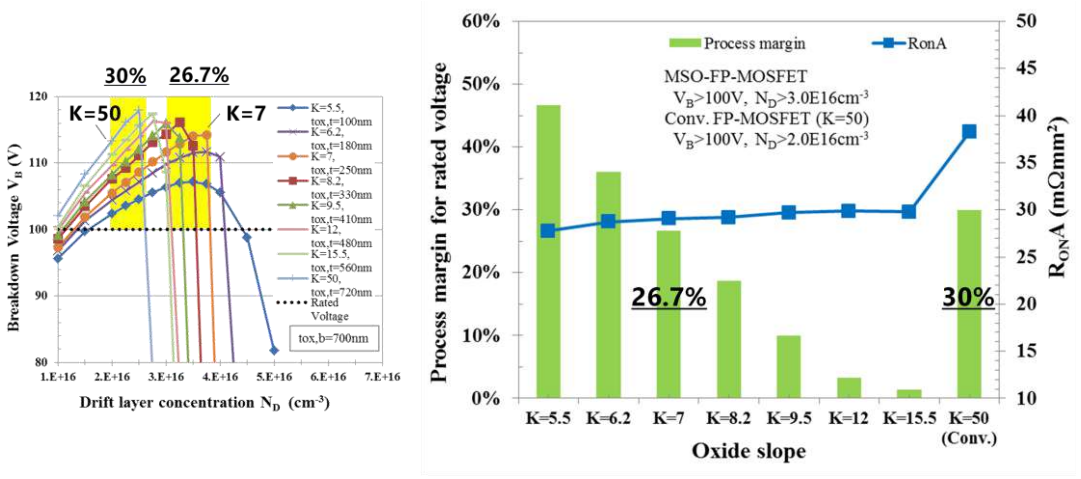


Fig. 3-32. Simulated K dependence of V_B process margin over 100 V. And K dependence of $R_{ON}A$; at N_D = 3.0×10^{16} /cm^3 for MSO-FP-MOSFETs and at N_D = 2.0×10^{16} /cm^3 for conventional FP-MOSFET. Reconstructed from Fig. 3-29 and Fig. 3-31. [73] (modified).

Fig. 3-32 shows the simulated V_B process margin and the $R_{ON}A$ at the N_D with the V_B margin maintained, for the MSO-FP-MOSFETs and the conventional FP-MOSFET. Those data can read from Fig. 3-29 and Fig. 3-31, and shown as the K dependence. The V_B process margin represents a range that satisfies both V_B > 100 V and N_D > 3.0×10^{16} /cm^3 for the MSO-FP-MOSFETs; or both V_B > 100 V and N_D > 2.0×10^{16} /cm^3 for the conventional FP-MOSFET.

The V_B margin to maintain over 100 V of the conventional FP-MOSFET is 30%. In the MSO-FP-MOSFET, it is found that the smaller the K, the larger the V_B margin. When the K is 7, 26.7% margin, which is approximately same as the conventional one, is maintained.

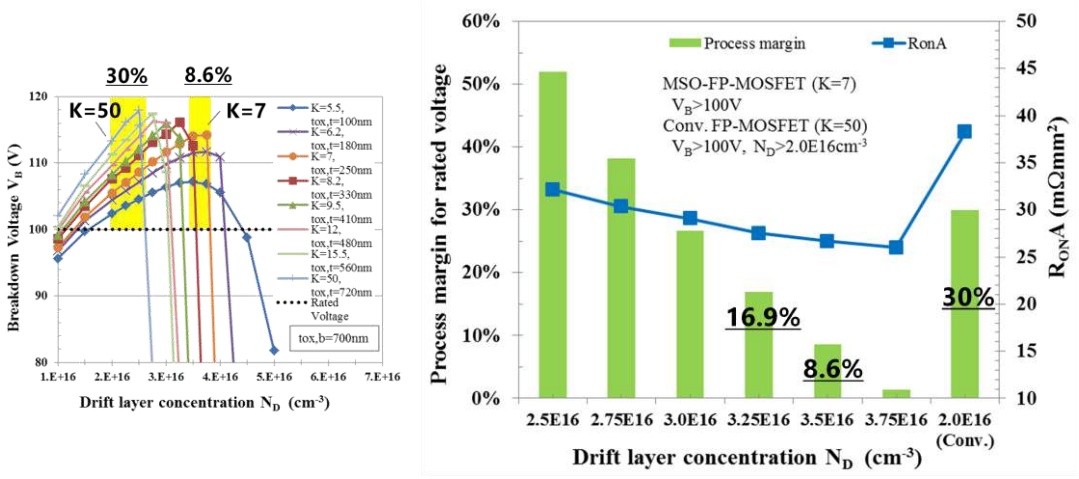


Fig. 3-33. Simulated N_D dependence of V_B process margin up to 100 V and $R_{ON}A$ for MSO-FP-MOSFETs and conventional FP-MOSFETs. Reconstructed from Fig. 3-29 and Fig. 3-31. [73] (modified).

Fig. 3-33 shows the simulated V_B process margin over 100 V and the $R_{ON}A$, at K = 7 for the MSO-FP-MOSFETs, and at K = 50 for the conventional FP-MOSFET. Those data can read from Fig. 3-29 and Fig. 3-31, and shown as the N_D dependence. The V_B process margin represents a range that satisfies only V_B > 100 V for the MSO-FP-MOSFETs; or both V_B > 100 V and N_D > 2.0×10^{16} /cm^3 for the conventional FP-MOSFET.

If the higher N_D, which means the V_B process margin decrease, is permitted, it is possible to decrease the $R_{ON}A$ more. For example, when the margin is 16.9%, V_B = 112.9 V and $R_{ON}A$ = 27.5 mΩ·mm^2 can be obtained, or when the margin is 8.6%, V_B = 114.1 V and $R_{ON}A$ = 26.7 mΩ·mm^2 can be obtained

As mentioned above, the V_B process margin was discussed about the N_D, however, the tolerance of other parameters such as T_{FPOX_b}, T_{FPOX_t}, and W_{Mesa} have to be considered in real device manufacturing.

3.3.3.3. Process flow and essential process evaluation

To realize the MSO-FP-MOSFET cell structure, two types of the fabrication process are proposed. They are named Stepped Oxide Deposition (SOD) process and Stepped Oxide Etch-off (SOE) process, respectively.

Fig. 3-34(a)–(h) shows the SOD process for the case of five-step field-plate structure.

(a) Trench forming by photo-lithography and reactive ion-etching (RIE), followed by first thin oxide film deposition by chemical vapor deposition (CVD).
(b) Sacrificial layer formation and etching it back down to first depth, followed by the first oxide film etching
(c) Second oxide film deposition and second sacrificial layer formation to second depth, followed by the second oxide film etching.
(d) Third oxide film deposition and third sacrificial layer formation to third depth, followed by the third oxide film etching.
(e) Fourth oxide film deposition and fourth sacrificial layer formation to fourth depth, followed by the fourth oxide film etching.
(f) Fifth oxide film deposition and fifth sacrificial layer formation to fifth depth, followed by the fifth oxide film etching.
(g) The sacrificial layer etching, followed by gate oxidation.
(h) Poly-silicon deposition as gate electrode.

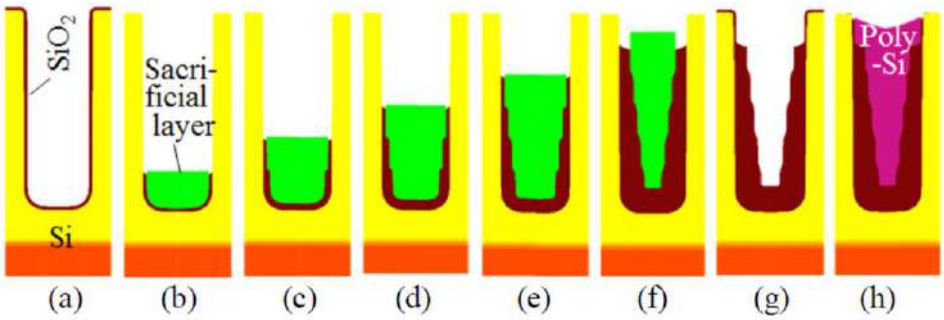


Fig. 3-34. Part of fabrication process flow of MSO-FP-MOSFET, named Stepped Oxide Deposition (SOD) process. (From trench formation to field-plate formation.) [72] © 2015 IEEE, [73].

After the process step (h), followed by p–base / n^+–source formation, inter-layer insulating film deposition, contact hole etching, metallization for source electrode, and back-surface metal formation for drain electrode.

Fig. 3-35(a)–(h) shows the SOE process for the case of five-step field-plate structure.

(a) Trench forming by photo-lithography and reactive ion-etching (RIE), followed by first thick oxide film deposition by chemical vapor deposition (CVD).
(b) Sacrificial layer formation and etching it back to first depth, followed by the first oxide film etching
(c) The sacrificial layer etching to second depth, followed by second oxide film etching slightly
(d) The sacrificial layer etching to third depth, followed by third oxide film etching slightly
(e) The sacrificial layer etching to fourth depth, followed by fourth oxide film etching slightly
(f) The sacrificial layer etching to fifth depth, followed by fifth oxide film etching slightly
(g) The sacrificial layer etching, followed by gate oxidation.
(h) Poly-silicon deposition as gate electrode.

After the process step (h), followed by p–base / n^+–source formation, inter-layer insulating film deposition, contact hole etching, metallization for source electrode, and back-surface metal formation for drain electrode.

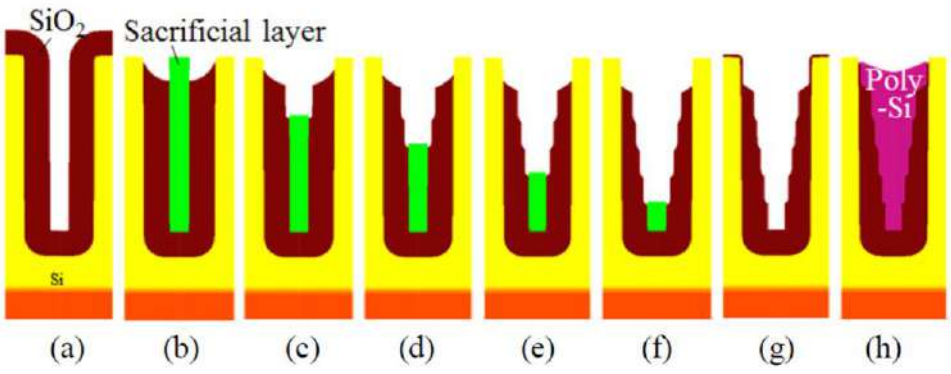


Fig. 3-35. Part of fabrication process flow of MSO-FP-MOSFET, named Stepped Oxide Etch-off (SOE) process. (From trench formation to field-plate formation.) [72] © 2015 IEEE, [73].

3.3.3.4. Experimental results of device performance

Fig. 3-36 shows cross-sectional SEM photograph of fabricated MSO-FP-MOSFET, which corresponds to field-plate (gate electrode) formation step of SOE process. It is observed that smooth four-step oxide and field-plate are formed successfully in 5.5-μm deep trench.

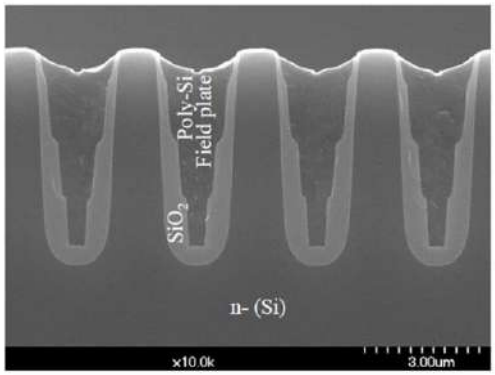


Fig. 3-36. Cross-sectional SEM photograph of fabricated MSO-FP-MOSFET, which corresponds to field-plate formation step of SOE process. [72] © 2015 IEEE, [73].

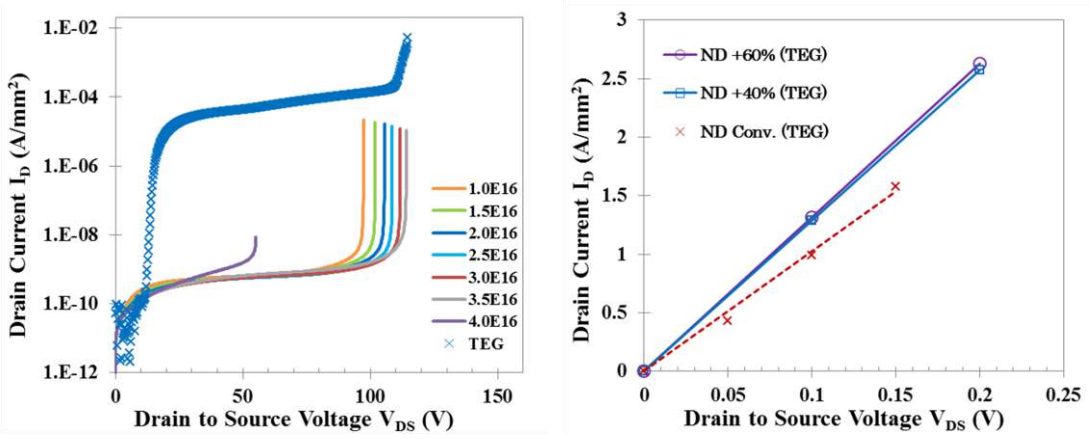
To demonstrate basic characteristics of the MSO-FP-MOSFET for the first time, test element group (TEG) having a diode and a resistance were fabricated on 3.73-mm^2 chip. As the diode TEG structure, p–base layer and p$^+$–contact layer were formed at top of n–drift layer of the surface of the mesa region. As the resistance TEG structure, n$^+$–contact layer were formed at top of n–drift layer of the surface of the mesa region. The poly-silicon, which acts as the field-plate, was connected to the source (anode) electrode.

In the evaluation samples, observed T_{FPOX_t} ($t_{OX,t}$), T_{FPOX_b} ($t_{OX,b}$) and W_{Mesa} were 310 nm, 580 nm and 1.4 μm, respectively.

By the diode TEG measurement, maximum V_B of 114.8 V was confirmed at approximately 1.5 times higher N_D than that of the conventional flat oxide structure, as shown in Fig. 3-37(a). However, the diode had a leakage current which was approximately five orders of magnitude higher than the simulated FP-MOSFET. This is because the device termination design was not optimized in this TEG.

On the other hand, by the resistance TEG measurement, 30% reduction of the on-current was confirmed under the condition of 40% higher N_D than that of the conventional flat oxide structure, as shown in Fig. 3-37(b). It is noted that there are differences between the resistance TEG and the MOSFET simulation; e.g., the TEG

includes a packaging resistance, the TEG does not include the channel resistance of the MOSFET that leads to R_{ON} increase, and the TEG does not include the accumulation effect of the MOSFET that leads to R_{ON} decrease.



(a) (b)

Fig. 3-37. (a) I_D–V_{DS} characteristics of the measured diode TEG, in comparison of the simulated MSO-FP-MOSFET. (b) I_D–V_{DS} characteristics of the measured resistivity TEG. [73]

3.3.4. Validation of on-resistance model

Fig. 3-38 shows the $R_{ON}A$ of simulated 100-V-class FP-MOSFETs (the conventional FP-MOSFET and the MSO-FP-MOSFET) compared with those of analytical model (the flat FP-MOSFET and the slant FP-MOSFET) in Eqs. (3-26)–(3-39). The structural parameters, electrical parameters, and physical constants are indicated in Table 3-7, Table 3-8, and Table 2-4.

In the case of the conventional/flat FP-MOSFETs, the $R_{ON}A$ at V_{gs} = 10 V calculated by the model is 37.5 mΩ·mm², which corresponds to the TCAD result of 37.5 mΩ·mm² completely. In the case of the slant/MSO-FP-MOSFETs, the $R_{ON}A$ at V_{gs} = 10 V calculated by the model is 28.2 mΩ·mm², which corresponds to the TCAD result of 28.4 mΩ·mm² with less than 1.0% error. It is noted that, in order to adjust to the model, $R_{N+}A$ component was subtracted from the $R_{ON}A$ of the original TCAD results.

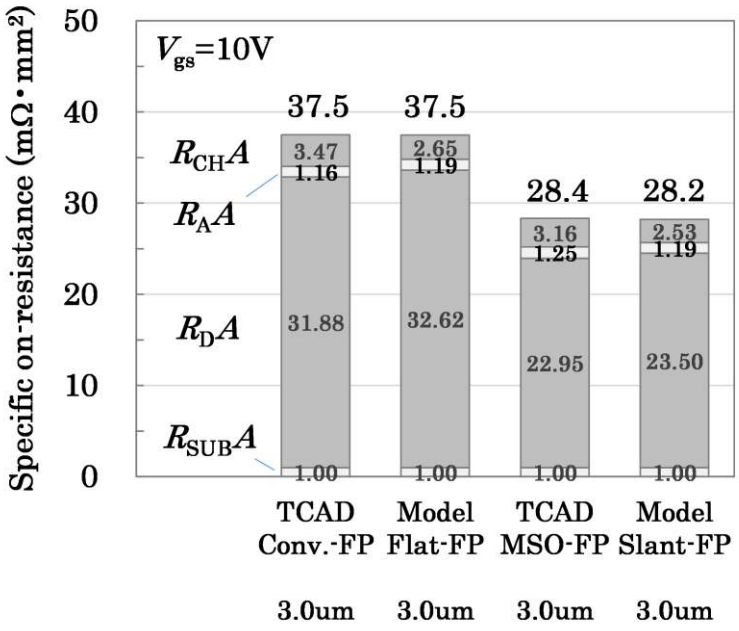


Fig. 3-38. $R_{ON}A$ of simulated 100-V-class FP-MOSFETs (conventional FP-MOSFET and MSO-FP-MOSFET) compared with those of analytical model (flat FP-MOSFET and slant FP-MOSFET). Under the condition of V_{gs} = 10 V.

Table 3-7. Structural parameters of 100-V-class FP-MOSFETs to calculate $R_{ON}A$.

Symbol	Parameters	Flat FP-MOSFET	MSO-FP-MOSFET	Unit
W_{Cell}	Cell width	3.00	3.00	μm
W_T	Trench width	1.80	1.80	μm
W_{Mesa}	Mesa width	1.20	1.20	μm
D_T	Trench depth	5.50	5.50	μm
L_{CH}	Channel length	0.30	0.30	μm
L_A	Accumulation length	0.20	0.20	μm
K_A	Coefficient of current spreading in the accumulation region	0.60	0.60	
T_{GOX}	Gate oxide thickness	0.075	0.075	μm
X_{JS}	n^+–Source junction depth	0.25	0.25	μm
X_{JB}	p–Base junction depth	0.55	0.55	μm
T_{FPOX}	Field-plate oxide thickness	0.70	N/A	μm
T_{FPOX_t}	Field-plate oxide thickness (top)	N/A	0.25	μm
T_{FPOX_b}	Field-plate oxide thickness (bottom)	N/A	0.70	μm
L_D	n–Drift layer length	4.95	4.95	μm
T_{BUF}	n–Buffer thickness	0.90	0.90	μm
ρ_D	Resistivity of n–drift layer	0.284	0.204	Ω・cm
N_D	Drift layer concentration	2.0×10^{16}	3.0×10^{16}	atoms/cm^3
T_{SUB}	n^+–Substrate thickness	50	50	μm
ρ_{SUB}	Resistivity of n^+–Substrate	0.0020	0.0020	Ω・cm
N_{SUB}	n^+–Substrate concentration	3.43×10^{19}	3.43×10^{19}	atoms/cm^3

Table 3-8. Electrical parameters of 100-V-class FP-MOSFETs to calculate $R_{ON}A$.

Symbol	Parameters	Flat FP-MOSFET	MSO-FP-MOSFET	Unit
V_{gs}	Gate–source voltage	10	10	V
V_{TH}	Threshold voltage	2.63	2.28	V
μ_{ni}	Electron mobility of inversion layer	500	500	cm^2/Vs
μ_{na}	Electron mobility of accumulation layer	550	550	cm^2/Vs
μ_{n_D}	Electron mobility of n–drift layer	1000	1000	cm^2/Vs
μ_{n_SUB}	Electron mobility of n^+–substrate	77.6	77.6	cm^2/Vs
V_{ON}	On-state voltage	0.10	0.10	V

3.3.5. 100-V two-step-oxide SFP-MOSFET [4]

3.3.5.1. Unit-cell structure design

In subsection 3.3.3, the MSO-FP-MOSFET, which is close to the ideal field-plate structure, was proposed. However, there is an issue which needs to the complicated process. Thus, in this subsection, a simplified field-plate structure is proposed. In addition, the source field-plate structure is applied to newly developed device to promise lower Q_{gd}, as mentioned in subsection 3.3.1 [74].

In Fig. 3-49, three kinds of FP-MOSFET structures are compared. The conventional FP-MOSFET has uniform field-plate oxide and straight poly-Si field-plate in the trench (Fig. 3-49(a)). This field-plate is connected to the source electrode at the termination region of the chip. This field-plate structure is standard in current commercial product. The MSO-FP-MOSFET is constructed by five-step oxide and tapered poly-Si field-plate (Fig. 3-49(b)). As shown in Fig. 3-49(c), proposed two-step FP-MOSFET is formed by two steps of thick oxide and two steps of field-plate poly-silicon to simplify the structure and fabrication process.

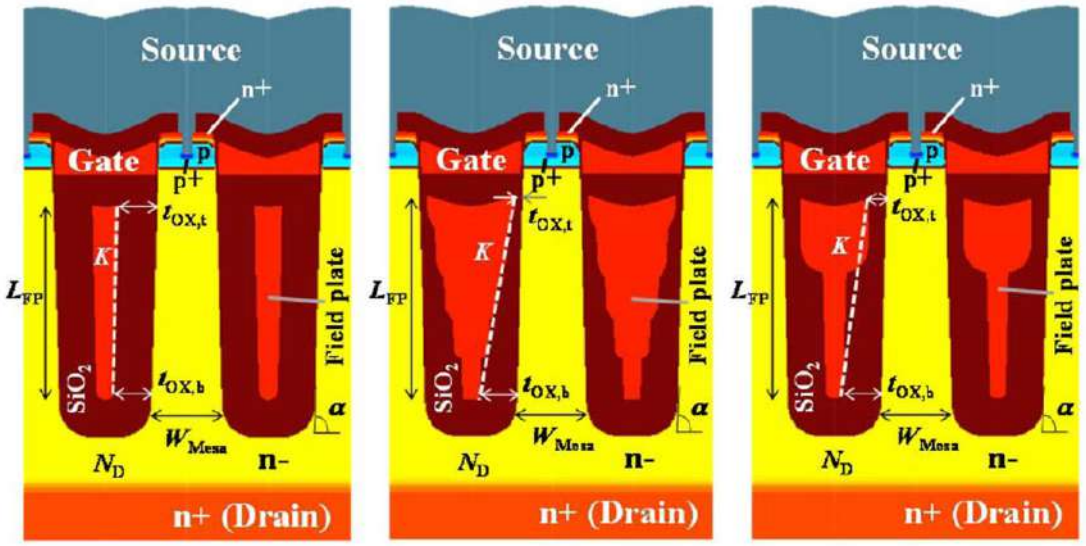


Fig. 3-39. Schematic cross-sectional structures of (a) conventional FP-MOSFET with uniform thick oxide, (b) multiple-stepped-oxide (MSO) FP-MOSFET, and (c) proposed 2-step FP-MOSFET. [74] (c) 2019 IEEE.

[4] Subsection 3.3.5 is reproduction of [74] chapter II–V, © 2019 IEEE, and a part of description is modified and comprehensive explanations are additionally provided.

3.3.5.2. Optimization of design parameters by TCAD simulation

As initial study for the three structures, off-state potential and electric field distribution are simulated. As design parameters, W_{Cell} = 3 μm, D_T = 5.5 μm, and N_D = 1×10^{16} – 3×10^{16} /cm^3 are chosen. Basically, the field plate inside the trench has effect to relax electric field in mesa region. Under the lower N_D condition (1×10^{16} /cm^3), approximately 100-V V_B is obtained for all three structures. However, Under the higher N_D condition (3×10^{16} /cm^3), as shown in Fig. 3-40, the V_B goes down to 52 V for the conventional FP-MOSFET because of high electric field at upper mesa region.

In contrary, both MSO and 2-step FP-MOSFETs realize over 110 V at the high N_D condition. Especially in the 2-step FP-MOSFET, it seems that the equipotential lines are approximately equal intervals. Also, the electric field is closer to uniform distribution. In a detail observation of the distribution, an inflection point at the oxide step position can be seen. As a result, it is found that the N_D can be designed to 1.5 times higher than conventional FP-MOSFET, which is the same effect as the MSO-FP-MOSFET as described in subsection 3.3.3.2.

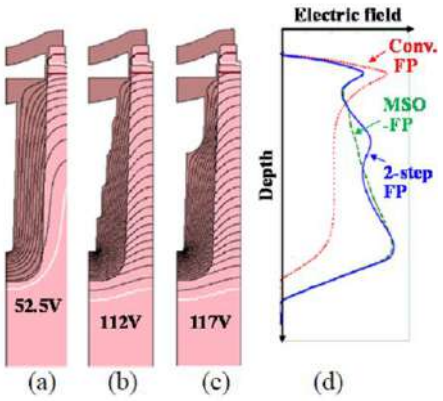


Fig. 3-40. Simulated 2-D potential contours (black lines), for (a) conventional, (b) MSO, and (c) 2-step FP-MOSFETs. (d) 1-D vertical electric field distributions along trench sidewall for conventional FP-MOSFETs (red dotted line), MSO-FP-MOSFETs (green dashed line), and 2-step FP-MOSFET (blue solid line). Under the condition of N_D = 3.0×10^{16} /cm^3. [74] (c) 2019 IEEE.

The field-plate oxide thickness at top position (T_{FPOX_t}) and at bottom position (T_{FPOX_b}) are considered as design parameter optimization. In Fig. 3-39, it is noted that the symbols T_{FPOX_t} and T_{FPOX_b} are expressed as $t_{OX,t}$ and $t_{OX,b}$. The field-plate oxide slope K is defined by Eq. (3-45). When the N_D, which can obtain a peak V_B ($V_{B,peak}$), is around

3.5×10^{16} – 3.75×10^{16} /cm^3, minimum $R_{ON}A$ can achieve at K = 8–9.7 in the 2-step FP-MOSFET.

Fig. 3-41 shows W_{Mesa} dependences of the $V_{B,peak}$ and "N_D at $V_{B,peak}$" for K = 9.2. The "N_D at $V_{B,peak}$" increases by decreasing W_{Mesa}. This is because an optimum charge is defined by the product of the N_D and the W_{Mesa}, as shown in Eq. (3-43). On the other hand, by increasing the W_{Mesa}, the V_B increases slightly. From these results, considering to easiness of fabrication process, the W_{Mesa} is selected to 1 μm, in following experiment.

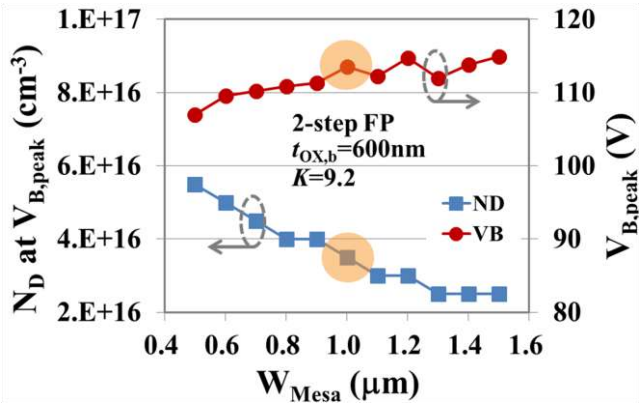


Fig. 3-41. Simulated W_{Mesa} dependences of $V_{B,peak}$ and "N_D at $V_{B,peak}$" for 2-step FP-MOSFETs. ($t_{OX,b}$ = 600 nm, K = 9.2). [74] © 2019 IEEE (modified).

3.3.5.3. Process flow and fabricated device structure

Representative process steps for the 2-step FP-MOSFET are shown in Fig. 3-42. (a) The trench of around 5.5-μm depth is formed by reactive ion etching (RIE), and followed by first thick oxidation. (b) By using sacrificial layer inside the trench, the thick oxide is etched down to approximately half-depth of the trench, and followed by second thick oxidation. (c) Polysilicon field-plate is formed by chemical vapor deposition (CVD) and RIE. (d) First interlayer oxide is filled in the trench by CVD and etched back to appropriate depth. (e) Gate oxidation and gate poly-silicon CVD are performed continuously. (f) The gate poly-silicon is etched. After that, following process steps such as p–base, n^+–source, p^+–body, second interlayer oxide, contact, surface metallization, wafer thinning and back-side metallization are performed.

Transmission Electron Microscope (TEM) photograph of a unit cell structure of fabricated 2-step FP-MOSFET is shown in Fig. 3-42(g). To relax a strong stress inside the trench during the gate poly-silicon forming, U-shaped gate structure is applied.

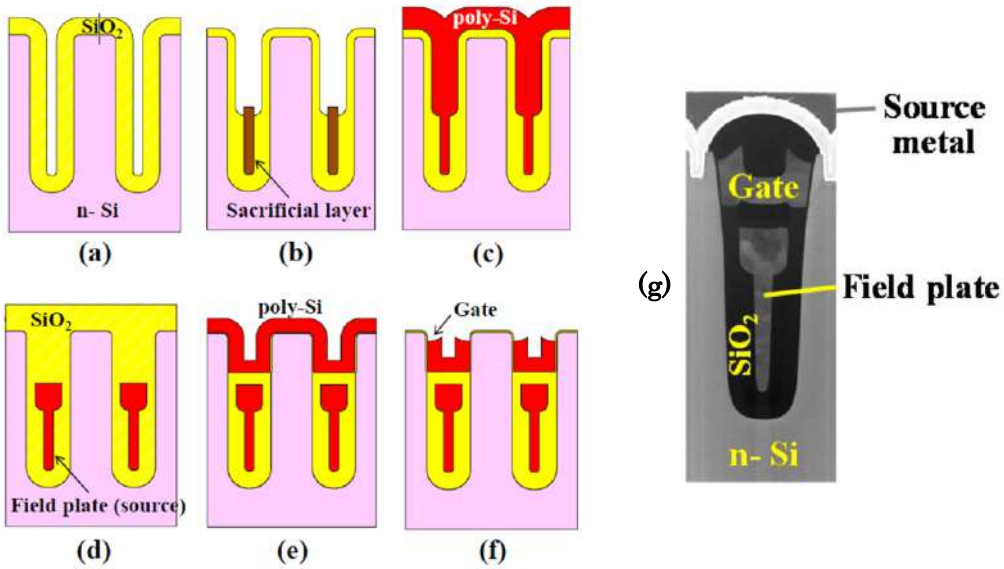


Fig. 3-42. (a)–(f) Part of fabrication process flow of 2-step FP-MOSFET (from thick oxide formation to gate electrode formation.). (g) TEM photograph of fabricated 2-step FP-MOSFET (unit cell). [74] (c) 2019 IEEE.

3.3.5.4. Experimental results of device performance

A. Breakdown voltage and on-resistance

In the fabricated 2-step FP-MOSFET, average of V_B at I_d = 10 mA was 109.9 V and the standard deviation was 0.50 V, with the target design and the center process conditions. R_{ON} packaged in 8-pin Small Outline Package (SOP-8) was measured under the condition of V_{gs} = 10 V and I_d = 30 A. The $R_{ON}A$ obtained by deduction of the package resistance indicated average value of 27.7 mΩ·mm² and good deviation of 0.46 mΩ·mm², as shown in Fig. 3-43. This $R_{ON}A$ of the 2-step FP-MOSFET is ultralow in ever reported 100-V-class device and improved by 16.6% compared with that of the conventional FP-MOSFET.

B. Figure-of-merit

When the FP-MOSFET is applied in high efficiency switching circuit, gate charge properties, i.e., gate–source charge (Q_{gs}), gate–drain charge (Q_{gd}), total gate charge (Q_g) and output charge (Q_{oss}), are very important. Moreover, as an indicator of the switching property, Q_{sw} is defined by sum of the Q_{gs} after threshold voltage and the Q_{gd}. Fig. 3-44 compares figure-of-merit (FOM) of the conventional and the 2-step FPMOSFET, under the conditions of V_{ds} = 50 V and I_d = 35 A as the gate charge measurement.

It was confirmed that $R_{ON}\cdot Q_g$ and $R_{ON}\cdot Q_{sw}$ were reduced by 27.1% and 4.7%, respectively, compared with those of the conventional device. The effect of the Q_g reduction includes modification of the gate–source insulating film structure in the fabricated device. On the other hand, $R_{ON}\cdot Q_{oss}$ was increased. The Q_{oss} is calculated by voltage integral of drain–source capacitance C_{ds}. In the 2-step FP-MOSFET, the N_D was increased to improve the $R_{ON}A$, so that depletion capacitance component of the C_{ds} was increased and it affected to the Q_{oss}. Thus, improvement of the tradeoff between $R_{ON}A$ and Q_{oss} is further challenge to realize ultimate FP-MOSFET.

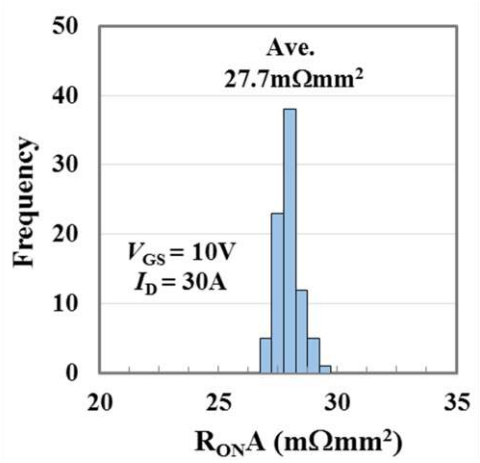


Fig. 3-43. Measured $R_{ON}A$ distribution of 2-step FP-MOSFETs fabricated by target design & center process conditions. [74] (c) 2019 IEEE.

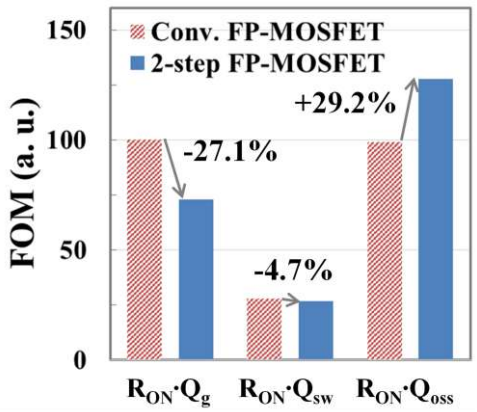


Fig. 3-44. Comparison of FOM for conventional and 2-step FP-MOSFETs. Measurement conditions: V_{gs} = 10 V and I_d = 30 A for R_{ON}, and V_{ds} = 50 V and I_d = 35 A for Q_g, Q_{sw}, and Q_{oss}. [74] (c) 2019 IEEE.

3.3.6. 18-V sub-micron cell pitch GFP-MOSFET

3.3.6.1. Unit-cell structure design

Applying the FP-MOSFET is expanding to improve the performances in wide range LV-MOSFETs. The lower the rated-voltage of MOSFET, the smaller the R_DA contribution. In short, the effect of the field-plate structure becomes small. In the lower voltage MOSFET such as 12–20-V, however, there is little room to reduce the $R_{ON}A$, in current advanced U-MOSFET technology, as shown in Fig. 3-45. Thus, each main component should be reduced as possible. As shown in Fig. 3-46, sub-micron cell pitch and the gate field plate are applied to an 18-V FP-MOSFET to reduce both $R_{CH}A$ and R_DA [75].

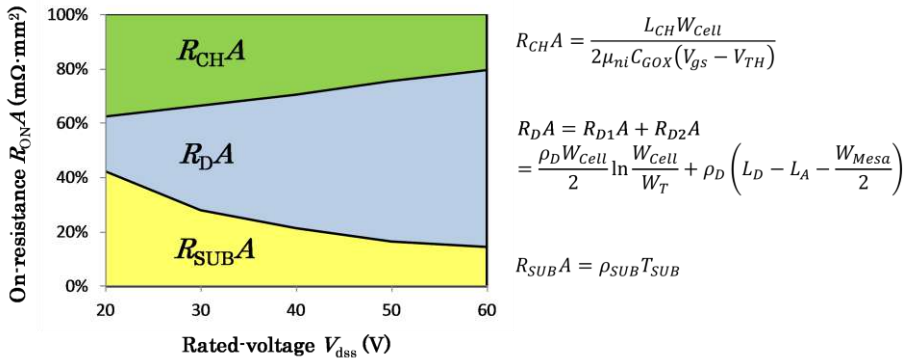
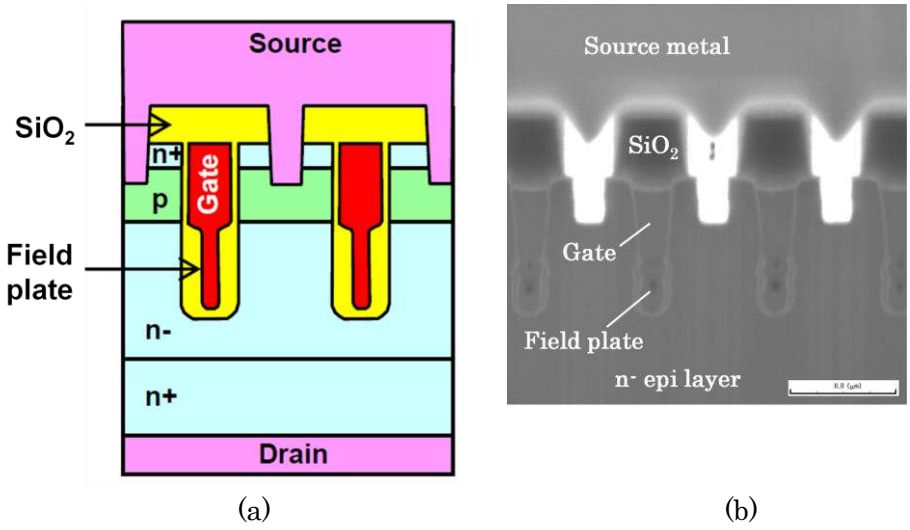


Fig. 3-45. Ratio of $R_{ON}A$ components for 20–60-V U-MOSFETs. [75] (modified).

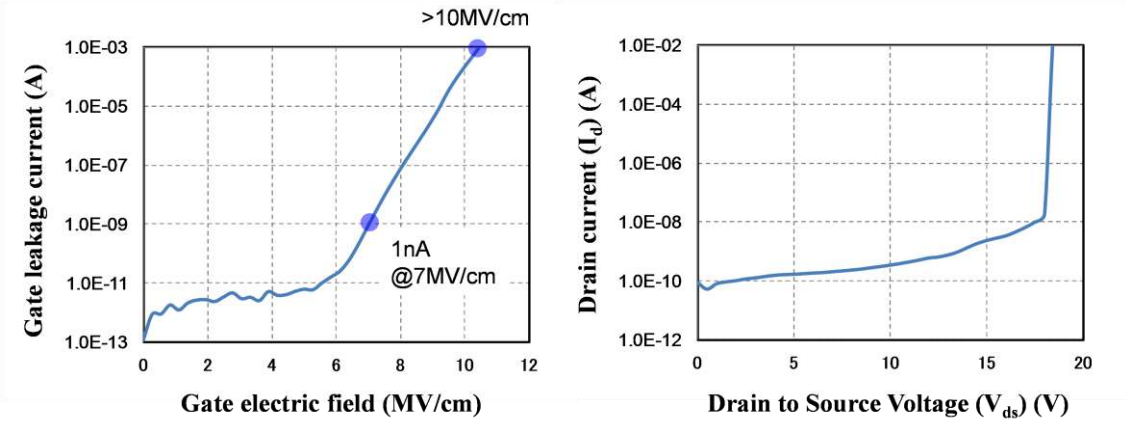


(a) (b)

Fig. 3-46. (a) Schematic cross-sectional structure and (b) SEM photograph of fabricated 18-V sub-micron cell pitch FP-MOSFET. [75] (modified).

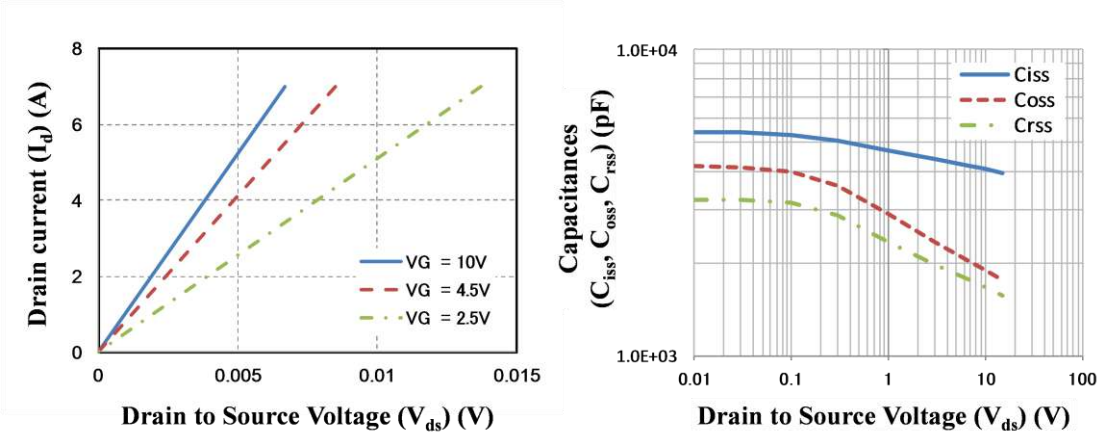
3.3.6.2. Experimental results of fabricated device

Representative characteristics of fabricated 0.92-μm-pitch 18-V FP-MOSFET are described below. Active area is 2.3 mm². The leakage current of the gate oxide was 1 nA at 7 MV/cm, and the electric field that leads to a breakdown was over 10 MV/cm. It showed ideal insulation properties and a smoothness of the connection between the gate oxide and the field-plate oxide (Fig. 3-47(a)). The V_B of 18 V (Fig. 3-47(b)), the $R_{ON}A$ of 2.1 mΩ·mm² at V_{gs} = 10 V and 2.6 mΩ·mm² at V_{gs} = 4.5 V were obtained (Fig. 3-48(a)). The capacitances as a function of the V_{ds} were showed in Fig. 3-48(b) for reference.



(a) (b)

Fig. 3-47. (a) Gate leakage current as a function of the gate electric field and (b) off-state I_d–V_{ds} characteristic of fabricated 18-V FP-MOSFET. [75] (modified).



(a) (b)

Fig. 3-48. (a) On-state I_d–V_{ds} characteristic [75] and (b) capacitances (C_{iss}, C_{oss}, and C_{rss}) as a function of V_{ds} of fabricated 18-V FP-MOSFET.

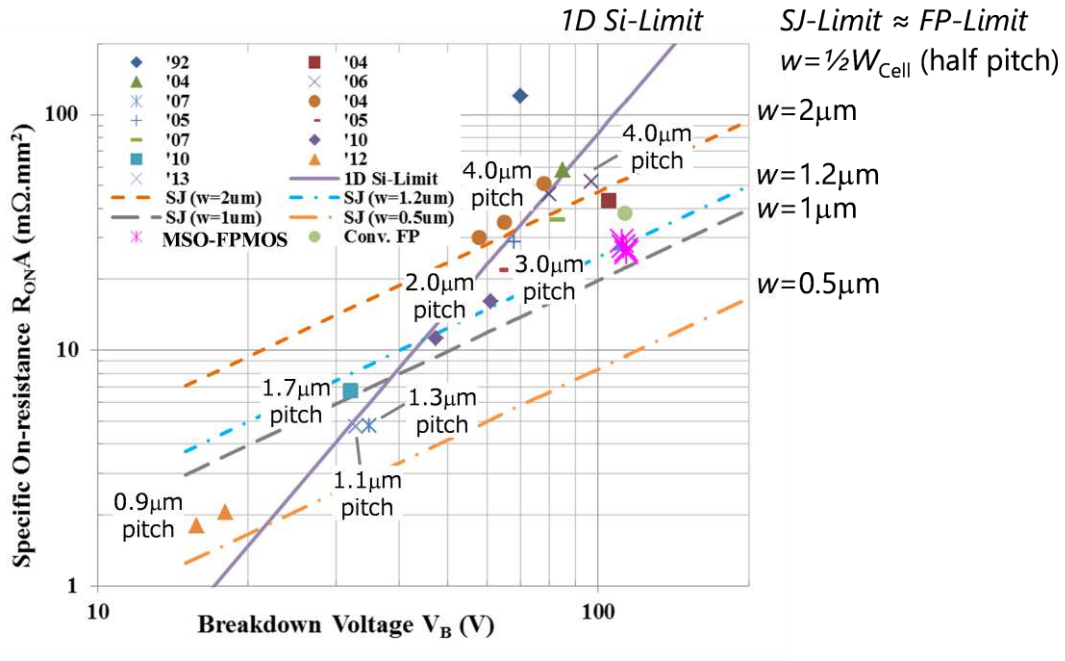
3.4. Summary

In chapter 3, superjunction U-MOSFET (SJ-UMOSFET) and field-plate U-MOSFET (FP-MOSFET), which are evolution structure of U-MOSFET, were described. The $R_{ON}A$ models of both SJ-UMOSFETs and FP-MOSFETs were detailed for three different surface patterns (stripe, square cell, and square p–column in stripe trench) in the SJ-UMOSFETs and four different structures (flat GFP, flat SFP, slant GFP, and slant SFP) in the FP-MOSFETs, respectively.

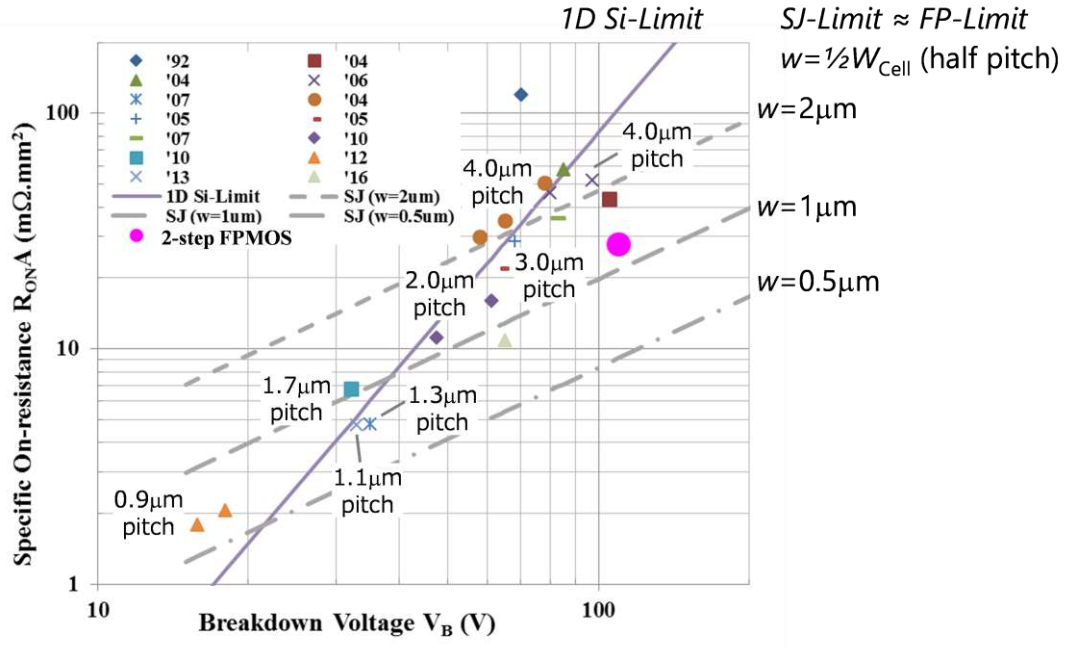
In addition, each improvement structure, fabrication process, and evaluation result of the fabricated devices were described. In the validation of the $R_{ON}A$ models, the real device and calculated results by the model were compared for both 60-V SJ-UMOSFET and 100-V FP-MOSFET, and it was confirmed they showed good agreement.

As a summary of the development of the novel SJ-UMOSFETs and FP-MOSFETs, the performances are compared each other. Fig. 3-49 shows the benchmarking of the tradeoff characteristics between the $R_{ON}A$ and the V_B for 18–100-V-class FP-MOSFETs [8] [49] [50] [51] [52] [71] and SJ-UMOSFETs [55] [56] [57] [76] by published data and author's research [10] [64] [72] [74] [75] [77]. As reference lines, 1-D silicon-limit [11] and SJ-limit [60] for half-cell pitch w = 2–0.5 μm are also indicated.

In the developed novel devices, which are the continuous p–column SJ-UMOSFET [10], the split p–column SJ-UMOSFET [64] [77], the MSO-GFP-MOSFET [72], the 2-step SFP-MOSFET [74], and the sub-micron-pitch GFP-MOSFET [75], superior performances were demonstrated against the published data.



(a)



(b)

Fig. 3-49. Tradeoff characteristics between $R_{ON}A$ and V_B for FP-MOSFETs and SJ-UMOSFETs; by published data [8] [49] [50] [51] [52] [55] [56] [57] [71] [76] and author's research [10] [64] [72] [74] [75] [77]. (a) Including 100-V MSO-FP-MOSFET and (b) including 100-V 2-step FP-MOSFET. [72] (modified).

4. Structure-Based Capacitance Modeling for the Latest FP-MOSFET Comparing with D-MOSFET

4.1. Overview of structure-based capacitance modeling

Several analytical capacitance models for different vertical power device structures have been reported, e.g., those for silicon D-MOSFETs [78], silicon U-MOSFETs [79] [80] [81], and silicon carbide (SiC) D-MOSFETs [82]. In those reports, however, since the C_{oss} components of D-MOSFETs and U-MOSFETs are relatively simple, those modeling methods are not applied to complex-structured FP-MOSFETs

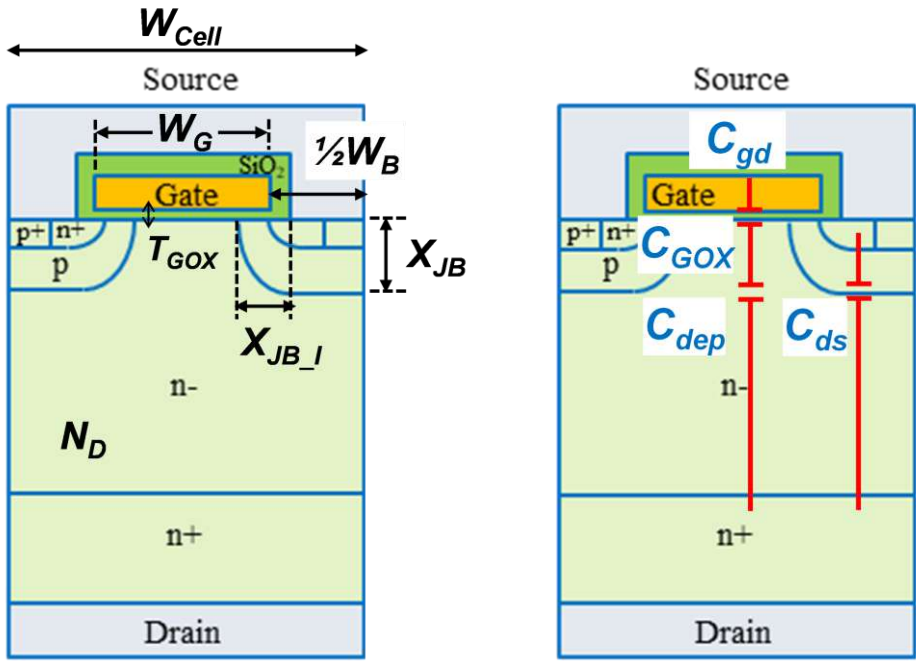
In this chapter, firstly, the capacitance model for the D-MOSFET is described. Subsequently, the capacitance model and the modeling method for the latest slant FP-MOSFET are detailed comprehensively.

4.2. D-MOSFET model

4.2.1. Structural parameters and basic characteristics for motif device

This subsection describes a 100-V-class D-MOSFET as a motive device for the capacitance modeling [83] [84]. Fig. 4-1(a) shows schematic cross section and representative structural parameters of the D-MOSFET to describe the capacitance model. Fig. 4-1(b) shows components of output capacitance (C_{oss}) and reverse transfer capacitance (C_{rss}) of the D-MOSFET.

The capacitance model can be described by structural parameters such as detailed cell structure dimensions and impurity doping concentrations, as shown in Table 4-1. It does not require any measurement of electrical characteristics. Physical constants used in the modeling are the same as those shown in Table 4-2. As shown in Table 4-1, the unit cell width (W_{Cell}) of the D-MOSFET is set to 6.0 μm, which can be obtained the V_B of 100 V, as described later.



(a) (b)

Fig. 4-1. (a) Schematic cross sections and representative structural parameters of D-MOSFET. (b) Components of output capacitance (C_{oss}) and reverse transfer capacitance (C_{rss}) for D-MOSFET. [83] [84] Copyright (2018) The Japan Society of Applied Physics.

Table 4-1. Structural parameters of 100-V-class D-MOSFET to calculate capacitances. [84] (modified).

Symbol	Parameters	Numerics	Unit
W_{Cell}	Cell width	6.00	μm
W_G	Gate width	3.40	μm
W_B	p–Base width	2.60	μm
T_{GOX}	Gate oxide thickness	0.05	μm
X_{JB}	p–Base junction depth	0.75	μm
X_{JB_l}	p–Base junction lateral length	0.60	μm
N_D	Drift layer concentration	2.8×10^{15}	atoms/cm^3
N_A	p–Base layer concentration	5.0×10^{16}	atoms/cm^3

Table 4-2. Physical constants to calculate capacitances.

Symbol	**Description**	**Property**	**Unit**
q	Elementary charge	1.60×10^{-19}	C
k	Boltzmann's constant	1.38×10^{-23}	J/K
T	Absolute temperature	300	K
n_i	Intrinsic carrier density	1.50×10^{10}	atoms/cm^3
ε_0	Permittivity in vacuum	8.854×10^{-14}	F/cm
ε_{Si}	Dielectric constant of Si	11.7	
ε_{OX}	Dielectric constant of SiO_2	3.9	

Before the capacitance modeling, basic characteristics of D-MOSFET was confirmed using the TCAD simulator named Sentaurus Device [85]. As a result, the D-MOSFET showed a sufficient V_B of 111.3 V and an $R_{ON}A$ of 199.1 mΩ·mm^2, as shown in Table 4-3.

Table 4-3. TCAD simulated basic characteristics for 100-V-class D-MOSFET. [84] (modified).

Symbol	Characteristics	Conditions		Unit
V_{Bs}	Breakdown voltage	J_d = 1μA/mm^2	111.3	V
V_{TH}	Threshold voltage	V_{ds} = 10 V, J_d = 1mA/mm^2	2.09	V
$R_{ON}A$	On-resistance	V_{gs} = 10 V, V_{ds} = 0.1 V	199.1	mΩ·mm^2
$R_{ON}\cdot C_{rss}$	FOM_1	V_{ds} = 50 V	1364	mΩ·pF
$R_{ON}\cdot C_{oss}$	FOM_2	V_{ds} = 50 V	4205	mΩ·pF
$R_{ON}\cdot Q_{oss}$	FOM_3	V_{ds} = 50 V	390	mΩ·pF

4.2.2. Components of output capacitance (C_{oss}) [5]

Fig. 4-1(b) shows the components of C_{oss} in the D-MOSFET. C_{oss} is simply expressed as sum of drain–source capacitance C_{ds} and gate–drain capacitance C_{gd}.

$$C_{oss}{}^{DMOS} = C_{ds} + C_{gd} \tag{4-1}$$

4.2.3. Drain–source capacitance (C_{ds})

The C_{ds} is a pn-junction capacitance and it is varied by the drain–source voltage V_{ds}.

$$C_{ds} = \sqrt{\frac{qN_D\varepsilon_{Si}\varepsilon_0}{2(V_{ds}+V_{bi})}} \cdot \frac{(W_B + 2X_{JB\_l})}{W_{Cell}} \tag{4-2}$$

Here, q is the elementary charge, $\varepsilon_{Si}\varepsilon_0$ is the permittivity of silicon, W_B is the p–base width, and X_{JB_l} is the lateral expansion length of the p–base junction. The built-in potential V_{bi} is given by

$$V_{bi} = \frac{kT}{q}\ln\frac{N_A N_D}{{n_i}^2}, \tag{4-3}$$

where k is Boltzmann's constant, T is the absolute temperature, n_i is the intrinsic carrier density of Si, and N_A is a p–base layer concentration.

4.2.4. Gate–drain capacitance (C_{gd})

The C_{gd} is a series connection of a gate oxide capacitance (C_{GOX}) and a depletion layer capacitance (C_{dep}). Since C_{rss} is equal to C_{gd}, C_{rss} is written as

$$C_{rss} = C_{gd} = \frac{C_{GOX}C_{dep}}{C_{GOX}+C_{dep}}. \tag{4-4}$$

Furthermore, C_{GOX} and C_{dep} are expressed as

$$C_{GOX} = \frac{\varepsilon_{OX}\varepsilon_0}{T_{GOX}} \cdot \frac{(W_G - 2X_{JB\_l})}{W_{Cell}}, \tag{4-5}$$

[5] Subsections 4.2.2–4.2.4 are reproduction of [84] section 3.1, Copyright (2018) The Japan Society of Applied Physics, and a part of description is modified.

$$C_{dep} = \frac{\varepsilon_{Si}\varepsilon_0}{W_{d\_mos}} \cdot \frac{(W_G - 2X_{JB\_l})}{W_{Cell}}, \tag{4-6}$$

where $\varepsilon_{OX}\varepsilon_0$ is the permittivity of SiO_2, T_{GOX} is the gate oxide thickness, and W_G is the gate width. W_{d_mos} is the depletion layer width beneath the gate electrode and is given by [86]

$$W_{d\_mos} = \frac{\varepsilon_{Si} T_{GOX}}{\varepsilon_{OX}} \left(\sqrt{\frac{2V_{ds}{\varepsilon_{OX}}^2 \varepsilon_0}{qN_D \varepsilon_{Si} {T_{GOX}}^2} + 1} - 1 \right). \tag{4-7}$$

By substituting Eqs. (4-5)–(4-7) into Eq. (4-4), the C_{rss} model can be obtained.

$${C_{rss}}^{DMOS} = C_{gd} = \frac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\frac{2V_{ds}{\varepsilon_{OX}}^2 \varepsilon_0}{qN_D \varepsilon_{Si}} + {T_{GOX}}^2}} \cdot \frac{W_G - 2X_{JB\_l}}{W_{Cell}} \tag{4-8}$$

Finally, by substituting Eqs. (4-2), (4-3) and (4-8) into Eq. (4-1), the C_{oss} model can be obtained.

$${C_{oss}}^{DMOS} = \sqrt{\frac{qN_D \varepsilon_{Si} \varepsilon_0}{2\left(V_{ds} + \frac{kT}{q} \ln \frac{N_A N_D}{{n_i}^2}\right)}} \cdot \frac{W_B + 2X_{JB\_l}}{W_{Cell}} + \frac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\frac{2V_{ds}{\varepsilon_{OX}}^2 \varepsilon_0}{qN_D \varepsilon_{Si}} + {T_{GOX}}^2}} \cdot \frac{W_G - 2X_{JB\_l}}{W_{Cell}} \tag{4-9}$$

4.2.5. List of capacitance model

Table 4-4. List of C_{oss} and C_{rss} model equations for D-MOSFET. [84] (modified).

${C_{rss}}^{DMOS} = \frac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\frac{2V_{ds}{\varepsilon_{OX}}^2 \varepsilon_0}{qN_D \varepsilon_{Si}} + {T_{GOX}}^2}} \cdot \frac{W_G - 2X_{JB\_l}}{W_{Cell}}$
${C_{oss}}^{DMOS} = \sqrt{\frac{qN_D \varepsilon_{Si} \varepsilon_0}{2\left(V_{ds} + \frac{kT}{q} \ln \frac{N_A N_D}{{n_i}^2}\right)}} \cdot \frac{W_B + 2X_{JB\_l}}{W_{Cell}} + {C_{rss}}^{DMOS}$

4.3. FP-MOSFET model

4.3.1. Structural parameters and basic characteristics for motif device

This subsection describes a 100-V-class slant FP-MOSFET which is the latest LV-MOSFET structure, as a motive device for the capacitance modeling [83] [84]. Fig. 4-2(a) shows schematic cross section and representative structural parameters of the slant FP-MOSFET. Fig. 4-2(b) shows comprehensive structural parameters of the slant FP-MOSFET to describe the capacitance model.

The capacitance model can be described by structural parameters such as detailed cell structure dimensions and impurity doping concentrations, as shown in Table 4-5. It does not require any measurement of electrical characteristics. Physical constants used in the modeling are the same as those shown in Table 4-2. As shown in Table 4-5, the unit cell width (W_{Cell}) of the FP-MOSFET is set to 2.6 μm, which is smaller than that of

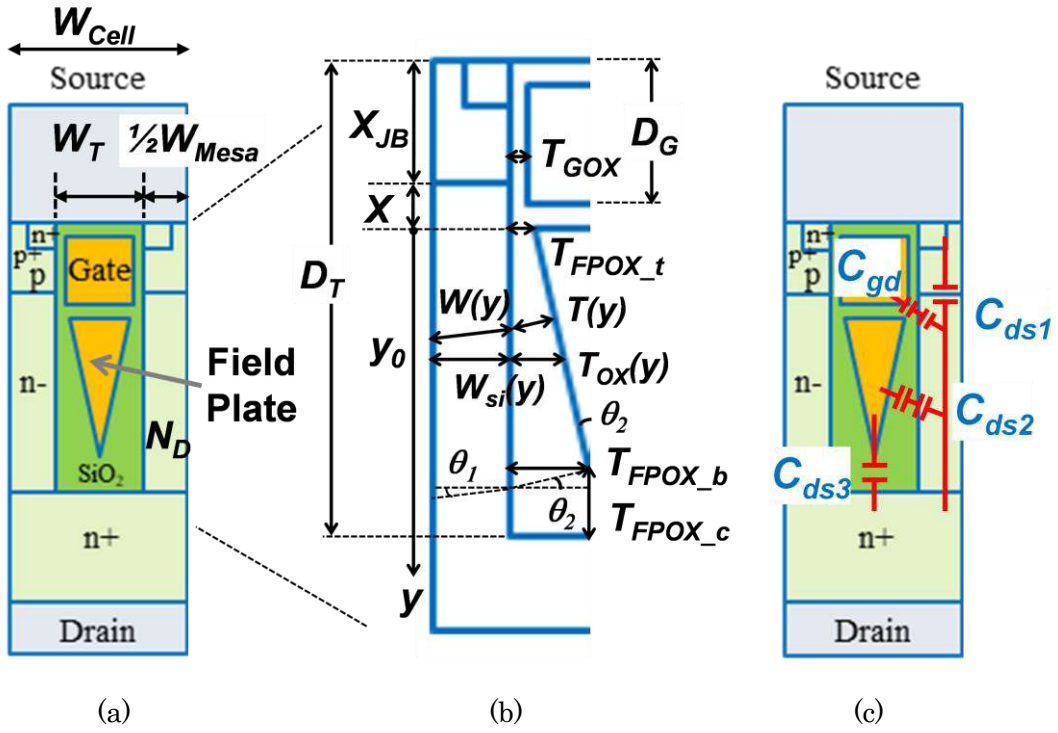


Fig. 4-2. (a) Schematic cross sections and representative structural parameters of slant FP-MOSFET. (b) Comprehensive structural parameters of FP-MOSFET (half-cell structure) to describe capacitance model. (c) Components of output capacitance (C_{oss}) and reverse transfer capacitance (C_{rss}) for FP-MOSFET. [83] [84] Copyright (2018) The Japan Society of Applied Physics.

D-MOSFET (6.0 μm) in subsection 4.2.1. Despite its smaller W_{Cell}, it has a drift layer concentration (N_D) that is ten times higher than that of the D-MOSFET.

Table 4-5. Structural parameters of 100-V-class FP-MOSFET to calculate capacitances. [84] (modified).

Symbol	Parameters	Numerics	Unit
W_{Cell}	Cell width	2.60	μm
W_T	Trench width	1.50	μm
W_{Mesa}	Mesa width	1.10	μm
D_T	Trench depth	6.00	μm
D_G	Gate depth	1.00	μm
T_{GOX}	Gate oxide thickness	0.05	μm
T_{FPOX_t}	Field-plate oxide thickness (top)	0.10	μm
T_{FPOX_b}	Field-plate oxide thickness (bottom)	0.75	μm
T_{FPOX_c}	Field-plate oxide thickness (center)	0.75	μm
X_{JB}	p–Base junction depth	0.90	μm
N_D	Drift layer concentration	3.0×10^{16}	atoms/cm^3
N_A	p–Base layer concentration	1.0×10^{17}	atoms/cm^3

Before the capacitance modeling, basic characteristics of the FP-MOSFETs were considered by using TCAD simulation as shown in Table 4-6. As a result, the FP-MOSFET showed a sufficient V_B of 110.1 V and an ultralow $R_{ON}A$ of 32.8 mΩ·mm^2, which was approximately one-sixth of that of the D-MOSFET, described in subsection 4.2.1. Moreover, in the FP-MOSET, a very small $R_{ON}\cdot C_{rss}$, which is approximately one-twentieth of that of the D-MOSFET, was confirmed. Those indicate good features of the FP-MOSFET. However, $R_{ON}\cdot Q_{oss}$ is still high. Therefore, the capacitance modeling especially for C_{oss}, which is required to the analysis of P_{Qoss}, is important.

Table 4-6. TCAD simulated basic characteristics for 100-V-class FP-MOSFET. [84] (modified).

Symbol	Characteristics	Conditions		Unit
V_B	Breakdown voltage	J_d = 1μA/mm^2	110.1	V
V_{TH}	Threshold voltage	V_{ds} = 10 V, J_d = 1mA/mm^2	2.03	V
$R_{ON}A$	On-resistance	V_{gs} = 10 V, V_{ds} = 0.1 V	32.8	mΩ·mm^2
$R_{ON}\cdot C_{rss}$	FOM_1	V_{ds} = 50 V	5.7	mΩ·pF
$R_{ON}\cdot C_{oss}$	FOM_2	V_{ds} = 50 V	2040	mΩ·pF
$R_{ON}\cdot Q_{oss}$	FOM_3	V_{ds} = 50 V	309	mΩ·pF

4.3.2. Components of the output capacitance (C_{oss}) [6]

As an approach to capacitance modeling in the complex FP-MOSFET structure, four components of C_{oss}, as shown in Fig. 4-2(c), are considered. The C_{oss} in the FP-MOSFET is simply expressed as

$$C_{oss}{}^{FPMOS} = C_{ds1} + C_{ds2} + C_{ds3} + C_{gd}. \tag{4-10}$$

Here, C_{ds1} is the depletion layer capacitance of the pn-junction, C_{ds2} is a series connection of a field-plate oxide capacitance and a depletion layer capacitance along the trench side wall, and C_{ds3} is the trench bottom capacitance including the field-plate oxide and depletion layers. In the FP-MOSFET, however, C_{gd} is negligible in the case of C_{oss} calculation, because the area of the parallel-plate capacitor is usually very small for optimized cell design.

Fig. 4-3 show the TCAD-simulated FP-MOSFET half-cell structures, which show the V_{ds} dependence of equal-potential contours. The potential contours of 5-V intervals and the depletion layer boundaries are shown as black and white lines, respectively. In each figure, the dominant capacitance components are C_{ds1}, C_{ds2}, and C_{ds3}, respectively.

4.3.3. pn-Junction capacitance

In the region of C_{ds1} (Fig. 4-3(a)), the depletion layer of the pn-junction extends down to the vertical direction with increasing V_{ds}. However, the capacitance width in the lateral direction decreases because of the expansion of another depletion layer along the trench side wall caused by the field-plate effect. It is considered that this pn-junction capacitance C_j is divided into C_{j0} and C_{j1} according to the V_{ds} condition.

$$C_{ds1} = C_j = \begin{cases} C_{j0}, & V_{ds} < 1(V) \\ C_{j1}, & V_{ds} \geq 1(V) \end{cases} \tag{4-11}$$

C_{j0} is the capacitance at an early voltage including the built-in potential V_{bi}. C_{j0} is modeled similarly to Eq. (4-2) for the C_{ds} of the D-MOSFET.

$$C_{j0} = \sqrt{\frac{qN_D\varepsilon_{Si}\varepsilon_0}{2(V_{ds}+V_{bi})}} \cdot \frac{W_{Mesa}}{W_{Cell}} \tag{4-12}$$

[6] Subsections 4.3.2–4.3.6 are reproduction of [84] section 3.2, Copyright (2018) The Japan Society of Applied Physics, and a part of description is modified and Eq. (29) is corrected.

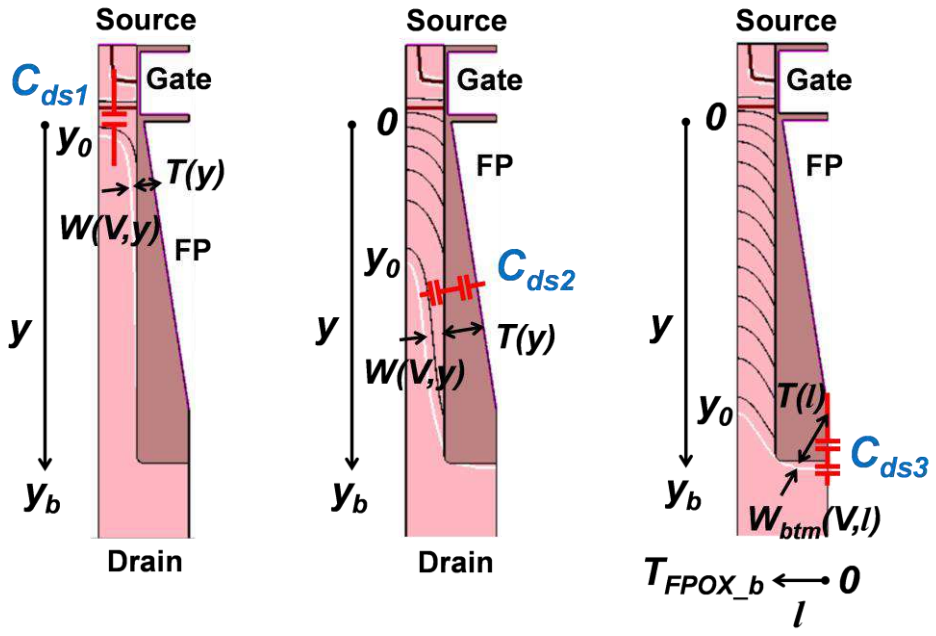


Fig. 4-3. TCAD-simulated FP-MOSFET half-cell structures, which represent V_{ds} dependence of equal-potential contours. Potential contours and depletion layer boundaries are shown as black lines and white lines, respectively. Three capacitance components are shown as dominant regions: (a) main pn-junction, (b) field-plate oxide and depletion layer along trench side wall, and (c) field-plate oxide and depletion layer of trench bottom. [84] Copyright (2018) The Japan Society of Applied Physics.

where W_{Mesa} is the mesa width, N_D is the n–drift layer concentration, and V_{bi} is the built-in potential.

Before C_{j1} modeling, some parameters shown in Fig. 4-2(b) are additionally explained. θ_2 is the angle of the field plate and it is given by

$$\theta_2 = \tan^{-1}\left(\frac{T_{FPOX\_b} - T_{FPOX\_t}}{D_T - X_{JB} - X - T_{FPOX\_c}}\right), \tag{4-13}$$

where T_{FPOX_t} and T_{FPOX_b} are the lateral field-plate oxide thicknesses at top and bottom positions, respectively, T_{FPOX_c} is the vertical field-plate oxide thickness of the center of the trench bottom, D_T is the trench depth, X_{JB} is the p–base junction depth, and X is the length between the X_{JB} and the horizontal position of the top of the field plate.

θ_l is the direction of the electric line of force and it is given by

$$\theta_1 = \tan^{-1}\left(\frac{\varepsilon_{Si}}{\varepsilon_{OX}}\tan\theta_2\right). \tag{4-14}$$

T(y) and *W(y)* are used to calculate the charge densities in the field-plate oxide and the silicon mesa region, respectively, and are given by

$$T(y) = T_{OX}(y)\cos\theta_2, \tag{4-15}$$

$$W(y) = \frac{W_{Si}(y)}{\cos\theta_1}, \tag{4-16}$$

where *y* is the depth from the top of the field plate, $T_{OX}(y)$ is the field-plate oxide thickness at the position *y* and $W_{Si}(y)$ is the depletion layer width of the mesa region along the slant field plate at the position *y*. $T_{OX}(y)$ is expressed as

$$T_{OX}(y) = \frac{T_{FPOX\_b} - T_{FPOX\_t}}{D_T - X_{JB} - X - T_{FPOX\_c}}y + T_{FPOX\_t}. \tag{4-17}$$

Although *W(y)* varies with V_{ds}, it has to be considered that V_{ds} is shared by the voltage of the field-plate oxide (V_{OX}) and the voltage of the silicon mesa (V_{Si}). The relationship between V_{OX}, V_{Si}, *T(y)*, and *W(y)* are expressed as

$$V_{ds} = V_{Si} + V_{OX}, \tag{4-18}$$

$$V_{Si} = \frac{1}{2}E_{Si}W(y), \tag{4-19}$$

$$V_{OX} = E_{OX}T(y), \tag{4-20}$$

$$\varepsilon_{Si}E_{Si}\cos\theta_1 = \varepsilon_{OX}E_{OX}\cos\theta_2, \tag{4-21}$$

$$E_{Si} = \frac{qN_D}{\varepsilon_{Si}\varepsilon_0}W(y), \tag{4-22}$$

where E_{Si} and E_{OX} are the electric field strengths of the silicon mesa region and field-plate oxide region, respectively. *W(y)* is derived by solving Eqs. (4-18)–(4-22). Since *y* varies with V_{ds}, *W(y)* is exactly expressed as $W(V_{ds},y)$ and can be described as

$$W(V_{ds},y) = -\frac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2}\cdot T(y) + \sqrt{\left(\frac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2}\cdot T(y)\right)^2 + \frac{2\varepsilon_{Si}\varepsilon_0}{qN_D}\cdot V_{ds}}. \quad (4\text{-}23)$$

C_{j1} includes the effect of capacitance width decrease by $W(V_{ds},y)$ and is described as

$$C_{j1} = \frac{\varepsilon_{Si}\varepsilon_0}{y_0 + X}\cdot\frac{W_{Mesa} - 2W(V_{ds},y)}{W_{Cell}}. \quad (4\text{-}24)$$

4.3.4. Oxide and depletion layer capacitance along field plate

In the region of C_{ds2} (Fig. 4-3(b)), the initial C_{ds2} is nearly equal to the field-plate oxide capacitance C_{FPOX}. With increasing V_{ds}, the mesa region is depleted linearly owing to the relation $y_0 \propto V_{ds}$ in the vertical direction, and the lateral depletion width under the position of y_0 expands gradually by $W(V_{ds},y)$. Thus, C_{ds2} is divided into two components according to the V_{ds} condition.

$$C_{ds2} = \begin{cases} C_{FPOX} , & V_{ds} < 1(V) \\ C_{FP}(V_{ds}), & V_{ds} \geq 1(V) \end{cases} \quad (4\text{-}25)$$

C_{FPOX} is provided by integrating field-plate oxide thickness in the depth direction.

$$C_{FPOX} = \frac{2\left(D_T - X_{JB} - X - T_{FPOX\_c}\right)\varepsilon_{OX}\varepsilon_0}{W_{Cell}\left(T_{FPOX\_b} - T_{FPOX\_t}\right)}\cdot ln\frac{T_{FPOX\_b}}{T_{FPOX\_t}} \quad (4\text{-}26)$$

At an arbitrary position y, the charge, which is across the field plate and the depletion layer in the mesa region, is defined as dQ. Differential equation of dQ expresses a voltage change of the drain–source electric charge and described as

$$\frac{dQ}{dV} = qN_D\frac{d}{dV}W(V_{ds},y). \quad (4\text{-}27)$$

The voltage dependence capacitance $C_{FP}(V_{ds})$ is provided by integrating Eq. (4-27) from y_0 to y_b, which is the end of the depletion layer and is described as

$$C_{FP}(V_{ds}) = \frac{2\cdot\int_{y_0}^{y_b} qN_D\frac{d}{dV}\left(W(V_{ds},y)\right)dy}{W_{Cell}}. \quad (4\text{-}28)$$

Finally, by substituting Eqs. (4-15), (4-17) and (4-23) into Eq. (4-28), $C_{FP}(V_{ds})$ can be obtained.

$$C_{FP}(V_{ds}) = \frac{2}{W_{Cell}}\int_{y_0}^{y_b} \frac{\varepsilon_{Si}\varepsilon_0}{\sqrt{\frac{{\varepsilon_{Si}}^2\cos^2\theta_1\left[T_{FPOX\_t}+\frac{y\left(T_{FPOX\_t}-T_{FPOX\_b}\right)}{X_{JB}+X+T_{FPOX\_b}-D_T}\right]^2}{{\varepsilon_{OX}}^2\cos^4\theta_2}+\frac{2\varepsilon_{Si}\varepsilon_0 V_{ds}}{qN_D}}}dy \quad (4\text{-}29)$$

4.3.5. Trench bottom capacitance

In the region of C_{ds3} (Fig. 4-3(c)), when V_{ds} increase, at last y_0 reaches almost the same depth as that of bottom of field plate. C_{ds2} decreases continuously in the model (Eqs. (4-25) and (4-29)). Therefore, the trench bottom capacitance C_{ds3} has to be included as a component of total C_{oss}.

In the trench bottom region, the depletion layer $W_{btm}(V_{ds},l)$ begins to expand slightly when V_{ds} is greater than approximately 60 V. $W_{btm}(V_{ds},l)$ can be described similarly to Eq. (4-23).

$$W_{btm}(V_{ds},l) = -\frac{\varepsilon_{Si}\cos\theta_3}{\varepsilon_{OX}\cos\theta_4}\cdot T(l) + \sqrt{\left(\frac{\varepsilon_{Si}\cos\theta_3}{\varepsilon_{OX}\cos\theta_4}\cdot T(l)\right)^2+\frac{2\varepsilon_{Si}\varepsilon_0}{qN_D}\cdot V_{ds}} \quad (4\text{-}30)$$

Here, l is the length from the center of the trench, $T(l)$ is the oxide thickness of the trench bottom, and θ_4 and θ_3 are given by

$$\theta_4 = \tan^{-1}\left(\frac{l}{T_{FPOX\_c}}\right), \quad (4\text{-}31)$$

$$\theta_3 = \tan^{-1}\left(\frac{\varepsilon_{Si}}{\varepsilon_{OX}}\tan\theta_4\right). \quad (4\text{-}32)$$

Thus, C_{ds3} is provided by integrating $W_{btm}(V_{ds},l)$ in the direction of the trench width from 0 to T_{FPOX_b} and is described as

$$C_{ds3} = \frac{2\cdot\int_0^{T_{FPOX\_b}} qN_D\frac{d}{dV}(W_{btm}(V_{ds},l))dl}{W_{Cell}}. \quad (4\text{-}33)$$

4.3.6. Gate–drain capacitance (C_{gd})

As mentioned above, in the FP-MOSFET, C_{gd} is negligible small, which is approximately two to three orders of magnitude lower than C_{oss}. However, to compare it with the D-MOSFET, simplified modeling for C_{gd} were carried out. As shown in Fig. 4-2(b), the C_{gd} of the FP-MOSFET is the series connection of C_{GOX} and C_{dep}, which is the same as in the case of the D-MOSFET. In the FP-MOSFET, C_{GOX} and C_{dep} are expressed as

$$C_{GOX} = \frac{\varepsilon_{OX}\varepsilon_0}{T_{GOX}} \cdot \frac{2\left(D_G - X_{JB}\right)}{W_{Cell}}, \tag{4-34}$$

$$C_{dep} = \frac{\varepsilon_{Si}\varepsilon_0}{W_{d\_mos}} \cdot \frac{2\left(D_G - X_{JB}\right)}{W_{Cell}}. \tag{4-35}$$

Here, D_G is the gate depth, X_{JB} is the p–base junction depth, and T_{GOX} is the gate oxide thickness.

By substituting Eqs. (4-7), (4-34), and (4-35) into Eq. (4-4), the initial capacitance C_{gd0} can be obtained as

$$C_{gd0} = \frac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\frac{2V_{ds}{\varepsilon_{OX}}^2\varepsilon_0}{qN_D\varepsilon_{Si}} + {T_{GOX}}^2}} \cdot \frac{2\left(D_G - X_{JB}\right)}{W_{Cell}}. \tag{4-36}$$

Unlike the D-MOSFET, in the FP-MOSFET, the capacitance width of C_{gd} is drastically reduced by the factor of $W(V_{ds},y)$, as shown in Eq. (4-23). Thus, finally, the C_{rss} model is described as

$$\begin{aligned} {C_{rss}}^{FPMOS} &= C_{gd0} \cdot \frac{W_{Mesa} - 2W(V_{ds},y)}{W_{Mesa}} \\ &= \frac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\frac{2V_{ds}{\varepsilon_{OX}}^2\varepsilon_0}{qN_D\varepsilon_{Si}} + {T_{GOX}}^2}} \cdot \frac{2\left(D_G - X_{JB}\right)}{W_{Cell}} \cdot \frac{W_{Mesa} - 2W(V_{ds},y)}{W_{Mesa}}. \end{aligned} \tag{4-37}$$

4.3.7. List of capacitance model

Table 4-7. List of C_{oss} and C_{rss} model equations for FP-MOSFET. [84] (modified).

$$C_{rss}{}^{FPMOS} = \frac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\frac{2V_{ds}{\varepsilon_{OX}}^2\varepsilon_0}{qN_D\varepsilon_{Si}} + {T_{GOX}}^2}} \cdot \frac{2\left(D_G - X_{JB}\right)}{W_{Cell}} \cdot \frac{W_{Mesa} - 2W(V_{ds}, y)}{W_{Mesa}}$$

$$W(V_{ds}, y) = -\frac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2} \cdot T(y) + \sqrt{\left(\frac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2} \cdot T(y)\right)^2 + \frac{2\varepsilon_{Si}\varepsilon_0}{qN_D} \cdot V_{ds}}$$

$$C_{oss}{}^{FPMOS} = C_{ds1} + C_{ds2} + C_{ds3} + C_{gd}$$

$$C_{ds1} = \begin{cases} C_{j0} = \sqrt{\frac{qN_D\varepsilon_{Si}\varepsilon_0}{2(V_{ds}+V_{bi})}} \cdot \frac{W_{Mesa}}{W_{Cell}} & , \quad V_{ds} < 1(V) \\ C_{j1} = \frac{\varepsilon_{Si}\varepsilon_0}{y_0 + X} \cdot \frac{W_{Mesa} - 2W(V_{ds}, y)}{W_{Cell}}, & V_{ds} \geq 1(V) \end{cases}$$

$$C_{ds2} = \begin{cases} C_{OX} = \frac{2\left(D_T - X_{JB} - X - T_{FPOX\_c}\right)\varepsilon_{OX}\varepsilon_0}{W_{Cell}\left(T_{FPOX\_b} - T_{FPOX\_t}\right)} \cdot ln\frac{T_{FPOX\_b}}{T_{FPOX\_t}}, & V_{ds} < 1(V) \\ C_{FP}(V_{ds}) = \frac{2 \cdot \int_{y_0}^{y_b} qN_D \frac{d}{dV}\left(W(V_{ds}, y)\right)dy}{W_{Cell}} & , \quad V_{ds} \geq 1(V) \end{cases}$$

$$W(V_{ds}, y) = -\frac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2} \cdot T(y) + \sqrt{\left(\frac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2} \cdot T(y)\right)^2 + \frac{2\varepsilon_{Si}\varepsilon_0}{qN_D} \cdot V_{ds}}$$

$$C_{ds3} = \frac{2 \cdot \int_0^{T_{FPOX\_b}} qN_D \frac{d}{dV}(W_{btm}(V_{ds}, l))dl}{W_{Cell}}$$

$$W_{btm}(V_{ds}, l) = -\frac{\varepsilon_{Si}\cos\theta_3}{\varepsilon_{OX}\cos\theta_4} \cdot T(l) + \sqrt{\left(\frac{\varepsilon_{Si}\cos\theta_3}{\varepsilon_{OX}\cos\theta_4} \cdot T(l)\right)^2 + \frac{2\varepsilon_{Si}\varepsilon_0}{qN_D} \cdot V_{ds}}$$

$C_{gd} \sim 0$

4.4. Comparison of SFP-MOSFET and GFP-MOSFET models

4.4.1. Structural parameters and basic characteristics for motif device

This subsection describes a comparison between source field-plate (SFP) and gate field-plate (GFP) MOSFETs (cf. subsection 3.3.1) regarding the capacitance modeling [87]. 60-V-class slant FP-MOSFET which is the latest LV-MOSFET structure is chosen as a motive device, which are shown in Fig. 4-4(a) and (b). Comprehensive structural parameters of both FP-MOSFETs to describe the capacitance model are shown in Fig. 4-4(c).

The capacitance model can be described by structural parameters such as detailed cell structure dimensions and impurity doping concentrations, as shown in Table 4-8. Physical constants used in the modeling are the same as those shown in Table 4-2.

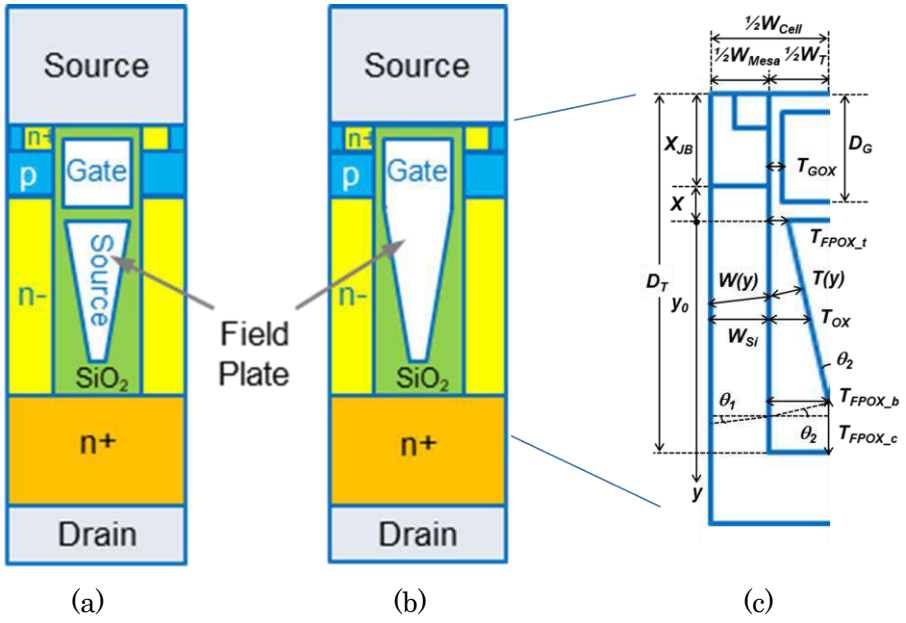


Fig. 4-4. Schematic cross-sectional structures for (a) SFP-MOSFET and (b) GFP-MOSFET. (c) Comprehensive structural parameters of FP-MOSFET (half-cell structure) to describe capacitance model. [87] (modified).

Table 4-8. Structural parameters of 60-V-class SFP/GFP-MOSFETs to calculate capacitances. [87] (modified).

Symbol	Parameters	Numerics	Unit
W_{Cell}	Cell width	1.60	μm
W_T	Trench width	0.80	μm
W_{Mesa}	Mesa width	0.80	μm
D_T	Trench depth	3.50	μm
D_G	Gate depth	1.00	μm
T_{GOX}	Gate oxide thickness	0.05	μm
T_{FPOX_t}	Field-plate oxide thickness (top)	0.05	μm
T_{FPOX_b}	Field-plate oxide thickness (bottom)	0.35	μm
T_{FPOX_c}	Field-plate oxide thickness (center)	0.40	μm
X_{JB}	p–Base junction depth	0.90	μm
N_D	Drift layer concentration	6.0×10^{16}	atoms/cm^3
N_A	p–Base layer concentration	2.2×10^{17}	atoms/cm^3

Before the comparison of capacitance model, basic characteristics of both FP-MOSFETs were simulated by TCAD. As a result in Table 4-9, both FP-MOSFETs showed a sufficient V_B of 67.4 V, and standard V_{TH} of 1.67–1.69 V, which can be driven by 5-V logic-level voltage. Ultralow $R_{ON}A$ of 10.9 mΩ·mm^2 and 8.7 mΩ·mm^2 were obtained for the SFP-MOSEFT and the GFP-MOSFET, respectively. The reason of the $R_{ON}A$ of the GFP-MOSFET which is 20% lower than that of the SFP-MOSFET is due to the smaller drift layer resistance R_DA, as shown in Eq. (3-30). In contrary, in the SFP-MOSET, a C_{rss} which is approximately two orders of magnitude lower than that of the GFP-MOSFET, was confirmed. Those indicate good features of both SFP-MOSFET and GFP-MOSFET.

Table 4-9. TCAD simulated basic characteristics for 60-V-class SFP/GFP-MOSFETs. [87] (modified).

Symbol	Characteristics	Conditions	SFP-MOSFET	GFP-MOSFET	Unit
V_B	Breakdown voltage	J_d = 1μA/mm^2	67.4	67.4	V
V_{TH}	Threshold voltage	V_{ds} = 10 V, J_d = 1mA/mm^2	1.69	1.67	V
$R_{ON}A$	On-resistance	V_{gs} = 10 V, V_{ds} = 0.1 V	10.9	8.70	mΩ·mm^2
C_{rss}/A	Input capacitance	V_{ds} = 30 V	821	827	pF/mm^2
C_{oss}/A	Output capacitance	V_{ds} = 30 V	147	147	pF/mm^2
C_{rss}/A	Reverse transfer capacitance	V_{ds} = 30 V	1.36	144	pF/mm^2

As described above, there is a possibility that the SFP-MOSFET and the GFP-MOSFET are selected according to the application. Therefore the capacitance modeling especially for both C_{oss} and C_{rss}, which are required to the analysis of P_{Qoss} and P_{SW}, are important.

4.4.2. Components of output capacitance (C_{oss}) and reverse transfer capacitance (C_{rss}) [7]

Fig. 4-5 shows parasitic capacitance components of both SFP-MOSFET and GFP-MOSFET, which are shown on the TCAD simulated unit cell structures.

Both C_{oss} and C_{rss} models for the SFP-MOSFET were described in section 4.3. It is considered that the capacitance components of the SFP-MOSFET can be replaced with those of the GFP-MOSFET.

For the SFP-MOSFET, the C_{oss} and the C_{rss} are given by

$$C_{oss}{}^{SFPMOS} = C_{ds1} + C_{ds2} + C_{ds3} + C_{gd}, \tag{4-38}$$

$$C_{rss}{}^{SFPMOS} = C_{gd}, \tag{4-39}$$

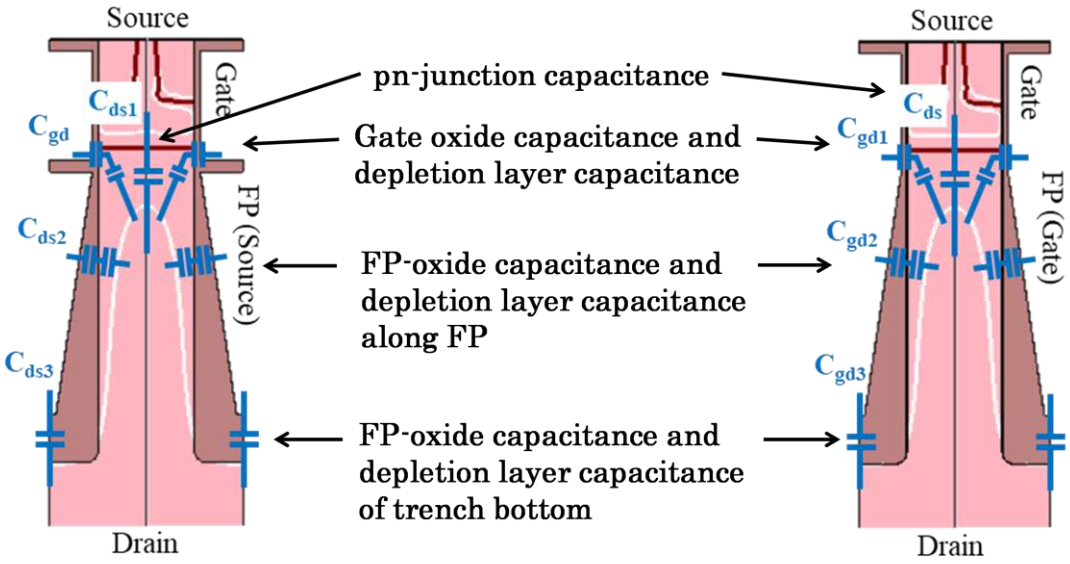
For the GFP-MOSFET, the C_{oss} and the C_{rss} are given by

$$C_{oss}{}^{GFPMOS} = C_{ds} + C_{gd1} + C_{gd2} + C_{gd3}, \tag{4-40}$$

$$C_{rss}{}^{GFPMOS} = C_{gd1} + C_{gd2} + C_{gd3}, \tag{4-41}$$

Regarding those components: C_{ds1}, C_{ds2}, C_{ds3}, C_{gd}, C_{ds}, C_{gd1}, C_{gd2}, and C_{gd3} are described in the following.

[7] Subsections 4.4.2–4.4.5 are reproduction of [87] chapter 3, and a part of description is modified and comprehensive explanations of the equations are additionally provided.



(a) (b)

Fig. 4-5. Parasitic capacitance components for (a) SFP-MOSFET and (b) GFP-MOSFET. White lines indicate depletion layer boundaries at V_{ds} = 10 V by TCAD simulation. [87] (modified).

4.4.3. pn-Junction capacitance

C_{ds1} of the SFP-MOSFET and C_{ds} of the GFP-MOSFET are expressed as same equation which is a pn-junction capacitance C_j of mesa region. In the region, the depletion layer of the pn-junction extends down to vertical direction of the drift layer as increasing V_{ds}. However, it is considered that this pn-junction capacitance C_j is divided into C_{j0} and C_{j1} according to the V_{ds} condition, as described in subsection 4.3.3. The C_j is given by the following in same manner to Eqs. (4-11)–(4-24).

$$C_{ds1} = C_{ds} = C_j = \begin{cases} C_{j0} = \sqrt{\dfrac{qN_D\varepsilon_{Si}\varepsilon_0}{2(V_{ds}+V_{bi})}} \cdot \dfrac{W_{Mesa}}{W_{Cell}}, & V_{ds} < 1.5\ (V) \\ C_{j1} = \dfrac{\varepsilon_{Si}\varepsilon_0}{y_0 + X} \cdot \dfrac{W_{Mesa} - 2W(V_{ds}, y)}{W_{Cell}}, & V_{ds} \geq 1.5\ (V) \end{cases} \quad (4\text{-}42)$$

Here, W_{Cell} is the cell width, W_{Mesa} is the mesa width, N_D is the n–drift layer concentration, V_{bi} is the built-in potential, y_0 is the depletion layer depth of center of the mesa, and X is the length between the p–base layer depth and the horizontal position of the top of the field plate.

In Eq. (4-42), $W(V_{ds},y)$ is the depletion layer width in the mesa region along the sloping field-plate, and is functional equation of the V_{ds} and y. Here, y is the depth from top of the field-plate. The $W(V_{ds},y)$ is expressed as below, which is the same as Eq. (4-23).

$$W(V_{ds},y) = -\frac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2}\cdot T(y) + \sqrt{\left(\frac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2}\cdot T(y)\right)^2 + \frac{2\varepsilon_{Si}\varepsilon_0}{qN_D}\cdot V_{ds}} \tag{4-43}$$

In Eq. (4-42), C_{j0} is the capacitance at an early voltage including the V_{bi}, and C_{j1} includes the effect of capacitance width decrease by $W(V_{ds},y)$. In the case of the 60-V-class FP-MOSFET, the boundary voltage between C_{j0} and C_{j1} is estimated as 1.5 V by TCAD simulation.

4.4.4. Gate–drain capacitance (C_{gd})

C_{gd} of the SFP-MOSFET and C_{gd1} of the GFP-MOSFET can be calculated as series connection of a gate oxide capacitance C_{GOX} and a depletion layer capacitance C_{dep}, and are described as

$$C_{gd} = C_{gd1} = \frac{C_{GOX}C_{dep}}{C_{GOX}+C_{dep}}. \tag{4-44}$$

Finally, both C_{gd} and C_{gd1} models are described as the following in same manner to Eq. (4-37).

$$C_{gd} = C_{gd1} = \frac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\frac{2V_{ds}{\varepsilon_{OX}}^2\varepsilon_0}{qN_D\varepsilon_{Si}} + {T_{GOX}}^2}}\cdot\frac{2\left(D_G - X_{JB}\right)}{W_{Cell}}\cdot\frac{W_{Mesa}-2W(V_{ds},y)}{W_{Mesa}}. \tag{4-45}$$

Here, D_G is the gate depth, X_{JB} is the p–base junction depth, and T_{GOX} is the gate oxide thickness.

4.4.5. Oxide and depletion layer capacitance along field plate

C_{ds2} of the SFP-MOSFET and C_{gd2} the GFP-MOSFET are also expressed as same equation of a series connection of the field-plate oxide and the depletion layer capacitance along the trench side wall.

In the region of C_{ds2} and C_{gd2} (Fig. 4-5), the initial capacitance is nearly equal to the field-plate oxide capacitance C_{FPOX}. With increasing the V_{ds}, the mesa region is depleted

gradually in lateral direction by the field-plate effect, and is linearly depleted in vertical direction. This capacitance is defined as the voltage dependence capacitance $C_{FP}(V_{ds})$ (cf. subsection 4.3.4).

Thus, both C_{ds2} and C_{gd2} are divided into two components according to the V_{ds} condition, and expressed as the following in same manner to Eqs. (4-25)–(4-29).

$$C_{ds2} = C_{gd2} = \begin{cases} C_{FPOX} = \dfrac{2\left(D_T - X_{JB} - X - T_{FPOX\_c}\right)\varepsilon_{OX}\varepsilon_0}{W_{Cell}\left(T_{FPOX\_b} - T_{FPOX\_t}\right)} \cdot ln\dfrac{T_{FPOX\_b}}{T_{FPOX\_t}}, & V_{ds} < 1.5\ (V) \\ C_{FP}(V_{ds}) = \dfrac{2 \cdot \int_{y_0}^{y_b} qN_D \dfrac{d}{dV}\left(W(V_{ds}, y)\right)dy}{W_{Cell}}, & V_{ds} \geq 1.5\ (V) \end{cases} \quad (4\text{-}46)$$

Here, D_T is the trench depth, T_{FPOX_t} and T_{FPOX_b} are the lateral field-plate oxide thicknesses at top and bottom positions, respectively, and T_{FPOX_c} is the vertical field-plate oxide thickness of the center of the trench bottom. Differential equation of $W(V_{ds},y)$ expresses a voltage change of the electric charge in the region.

4.4.6. Trench bottom capacitance

C_{ds3} of the SFP-MOSFET and C_{gd3} of the GFP-MOSFET are the trench bottom capacitance including the field-plate oxide and depletion layers. Both C_{ds3} and C_{gd3} models are described as the following in same manner to Eq. (4-33).

$$C_{ds3} = C_{gd3} = \frac{2 \cdot \int_0^{T_{FPOX\_b}} qN_D \dfrac{d}{dV}\left(W_{btm}(V_{ds}, l)\right)dl}{W_{Cell}} \quad (4\text{-}47)$$

Here, l is the length from the center of the trench and $T(l)$ is the oxide thickness of the trench bottom. In addition, the depletion layer of the trench bottom $W_{btm}(V_{ds},l)$ is given by Eq. (4-30).

C_{ds3} and C_{gd3} are simply calculated as 0.59 nF/cm^2.

4.4.7. List of capacitance model

Table 4-10. List of C_{oss} and C_{rss} model equations for SFP-MOSFET and GFP-MOSFET.

$C_{oss}{}^{SFPMOS} = C_{ds1} + C_{ds2} + C_{ds3} + C_{gd},$
$C_{rss}{}^{SFPMOS} = C_{gd},$
$C_{oss}{}^{GFPMOS} = C_{ds} + C_{gd1} + C_{gd2} + C_{gd3},$
$C_{rss}{}^{GFPMOS} = C_{gd1} + C_{gd2} + C_{gd3},$
$C_{ds1} = C_{ds} = C_j = \begin{cases} C_{j0} = \sqrt{\frac{qN_D\varepsilon_{Si}\varepsilon_0}{2(V_{ds}+V_{bi})}} \cdot \frac{W_{Mesa}}{W_{Cell}}, & V_{ds} < 1.5\ (V) \\ C_{j1} = \frac{\varepsilon_{Si}\varepsilon_0}{y_0 + X} \cdot \frac{W_{Mesa} - 2W(V_{ds}, y)}{W_{Cell}}, & V_{ds} \geq 1.5\ (V) \end{cases}$
$C_{ds2} = C_{gd2} = \begin{cases} C_{FPOX} = \frac{2(D_T - X_{JB} - X - T_{FPOX\_c})\varepsilon_{OX}\varepsilon_0}{W_{Cell}(T_{FPOX\_b} - T_{FPOX\_t})} \cdot ln\frac{T_{FPOX\_b}}{T_{FPOX\_t}}, & V_{ds} < 1.5\ (V) \\ C_{FP}(V_{ds}) = \frac{2 \cdot \int_{y_0}^{y_b} qN_D \frac{d}{dV}(W(V_{ds}, y))dy}{W_{Cell}}, & V_{ds} \geq 1.5\ (V) \end{cases}$
$C_{ds3} = C_{gd3} = \frac{2 \cdot \int_0^{T_{FPOX\_b}} qN_D \frac{d}{dV}(W_{btm}(V_{ds}, l))dl}{W_{Cell}}$
$C_{gd} = C_{gd1} = \frac{\varepsilon_{OX}\varepsilon_0}{\sqrt{\frac{2V_{ds}\varepsilon_{OX}{}^2\varepsilon_0}{qN_D\varepsilon_{Si}} + T_{GOX}{}^2}} \cdot \frac{2(D_G - X_{JB})}{W_{Cell}} \cdot \frac{W_{Mesa} - 2W(V_{ds}, y)}{W_{Mesa}}$

4.5. Summary

In chapter 4, components of the parasitic capacitances that are important to a switching loss design of the LV-MOSFET were described. The modeling for the latest slant FP-MOSFET, which structure was complicated, was studied in detail based on the D-MOSFET capacitance model. Output capacitance C_{oss} was divided into three elements (the pn-junction capacitance, the oxide film and depletion layer capacitance along the trench, and the oxide film and depletion layer capacitance of the trench bottom) of drain–source capacitance C_{ds} and the element of gate–drain capacitance C_{gd} in total. Each model equation was derived based on physical constants and device structural parameters.

5. Validation of Capacitance Model by Comparing Calculated MOSFET Characteristics and TCAD Simulations

5.1. 100-V-class D-MOSFET and FP-MOSFET [8]

As described in sections 4.2 and 4.3, the capacitances (C_{oss}, C_{rss}) for both D-MOSFET and FP-MOSFET can be modeled as shown in Table 4-4 and Table 4-7 [83] [84]. To validate an accuracy of the proposed model, some important characteristics related to the capacitances are compared between calculation by the model and TCAD simulation, which are using same structural parameters.

5.1.1. C_{oss}–V_{ds} curves

Firstly, C_{oss}–V_{ds} curves of the FP-MOSFET are calculated for each capacitance region. Fig. 5-1 shows the V_{ds} dependence of calculated C_{oss} and each component of the FP-MOSFET; C_j (= C_{j0} + C_{j1}), C_{FPOX}, $C_{FP}(V_{ds})$, and C_{ds3} are drawn as the capacitances of a unit device area (1 cm²).

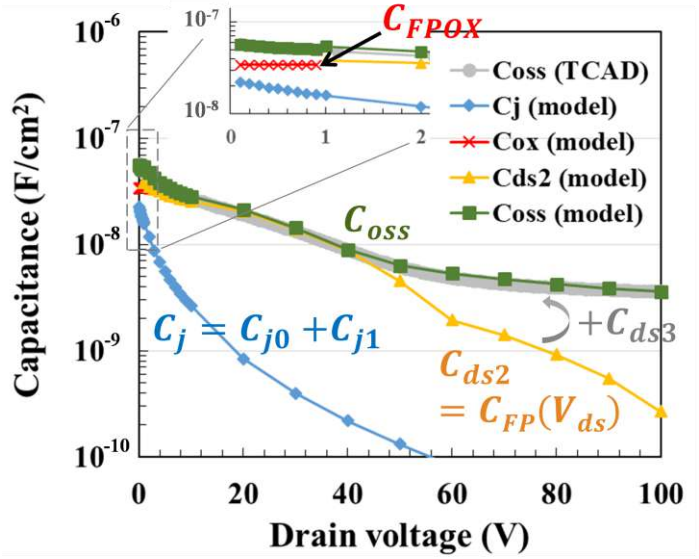


Fig. 5-1. C_{oss} components of 100-V-class FP-MOSFET calculated using proposed model compared with TCAD simulation results. [84] Copyright (2018) The Japan Society of Applied Physics.

[8] Section 5.1 is reproduction of [84] sections 4.1, 4.2 and 4.4, Copyright (2018) The Japan Society of Applied Physics, and a part of description is modified and comprehensive explanations are additionally provided.

In the low-voltage region of V_{ds} < 1V, C_j and C_{FPOX} were the dominant components of total C_{oss}, and the sum of C_j and C_{FPOX} corresponded well to TCAD results. This initial capacitance region is very important for calculating Q_{oss} and E_{oss}. The total C_{oss} curves, which consist of all components, in the region of $V_{ds} \geq$ 1V, also showed good agreement with TCAD results.

Then, C_{oss}–V_{ds} curves of both D-MOSFET and FP-MOSFET are compared. As described in subsections 4.2.1 and 4.3.2, it is obviously that the C_{oss} of the FP-MOSFET is larger than that of the D-MOSFET in the case of the same active area. However, each $R_{ON} \cdot C_{oss}$ is approximately same in both MOSFETs, as shown in Table 4-3 and Table 4-6. Therefore, each active area is calculated as considering the reduction effect of the R_{ON}.

The active area A is calculated considering 10% R_{ON} margin for the actual product design.

$$A = \frac{R_{ON}A}{R_{ON} \times 0.9} \tag{5-1}$$

Fig. 5-2(a) and (b) show the calculated C_{oss} for the D-MOSFET and the FP-MOSFET with TCAD simulation results, respectively. Here, each active area was designed to achieve same R_{ON} = 10 mΩ; therefore, 22.1 mm² for the D-MOSFET and 3.67 mm² for the FP-MOSFET were defined.

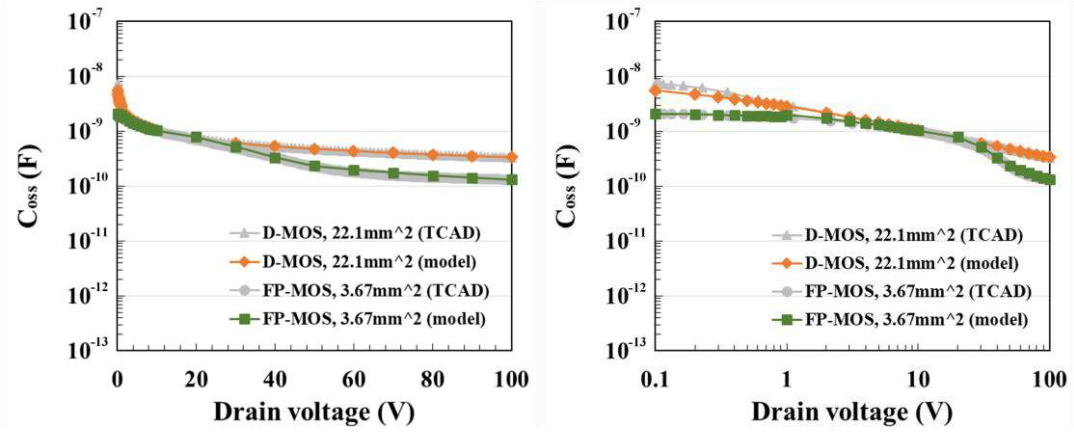


Fig. 5-2. C_{oss}–V_{ds} curves calculated using proposed model compared with TCAD results for 100-V-class D-MOSFET and FP-MOSFET. (a) V_{ds} linear scale and (b) V_{ds} log scale in X-axis. Each active area is designed for the same R_{ON} of 10mΩ. [84]

In both V_{ds} linear scale (Fig. 5-2(a)) and V_{ds} log scale (Fig. 5-2(b)), the C_{oss} curves of both MOSFETs corresponded well qualitatively to TCAD results. In the detailed comparison for the FP-MOSFET, errors of 14 and 10% were seen at approximately V_{ds} = 1 and 60 V, respectively, and another region showed less than 5%. These results indicate that the error occurred at the point where the V_{ds} condition changed, as shown in Eqs. (4-11), (4-25), and (4-33). In the D-MOSFET, a maximum error of 24% was seen at V_{ds} = 0.1 V; however, another region showed good results of less than 5%. The reason considered why the early voltage region has the error is that the spherical pn-junction of the p–base is not modeled very well.

5.1.2. Output charge (Q_{oss}) and stored energy (E_{oss})

By using the proposed model, the output charge Q_{oss} and the stored energy E_{oss} in the output capacitance are calculated as

$$Q_{oss} = \int C_{oss}(V_{ds})dV \tag{5-2}$$

$$E_{oss} = \int C_{oss}(V_{ds})V_{ds}dV \tag{5-3}$$

As mentioned above, this study especially focuses on the P_{Qoss} of the FP-MOSFET. Fig. 5-3(a) and (b) explain the switching operation concerning C_{oss}. When the MOSFET is turned-off, C_{oss} stores charges. Then, during the turn-on sequence, the on-current I_{ON} is consumed by discharging of Q_{oss}. This becomes the energy loss E_{oss}, which is the Q_{oss} loss of one switching cycle.

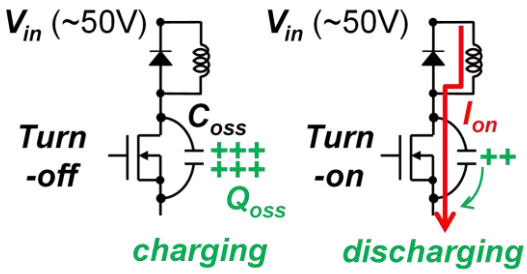
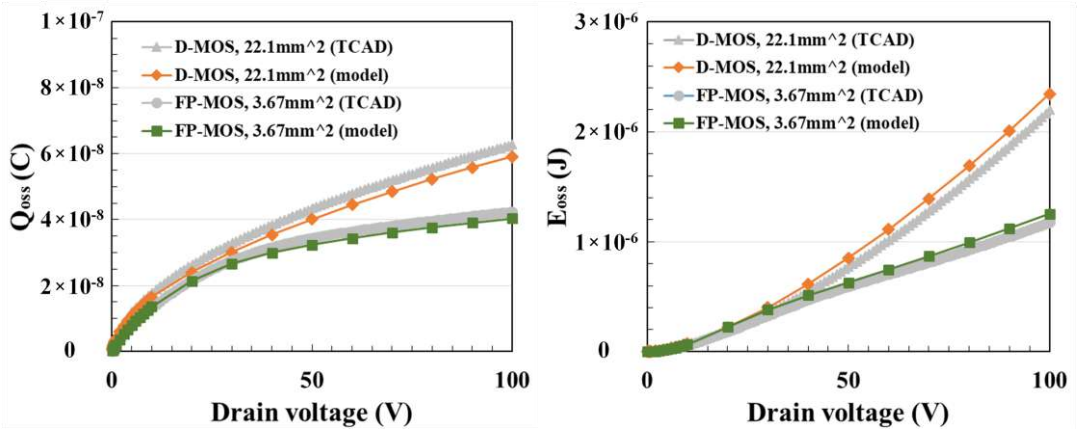


Fig. 5-3. Explanation of switching operation concerning C_{oss} and Q_{oss}. [84] Copyright (2018) The Japan Society of Applied Physics.

Fig. 5-4(a) and (b) show the calculated Q_{oss}–V_{ds} and E_{oss}–V_{ds} curves compared with TCAD simulation results, for the D-MOSFET and the FP-MOSFET, respectively. Each active area was designed for the same R_{ON} of 10 mΩ.

These modeled curves corresponded well qualitatively to TCAD curves. In an application circuit for 100-V-rating device, an input voltage (V_{IN}) of 50 V is assumed generally. In the comparison between the modeled Q_{oss} and the TCAD results at V_{ds} = 50 V, only 6 and 7% errors were seen for the FP-MOSFET and D-MOSFET, respectively. In addition, in the case of the E_{oss}, there were 5 and 10% errors for the FP-MOSFET and D-MOSFET, respectively. Therefore, it is recognized that these results are sufficient to use for power loss analysis.



(a) (b)

Fig. 5-4. (a) Q_{oss}–V_{ds} and (b) E_{oss}–V_{ds} curves calculated using proposed model compared with TCAD results for 100-V-class D-MOSFET and FP-MOSFET. Each active area is designed for the same R_{ON} of 10mΩ. [83] [84]

5.1.3. C_{rss}–V_{ds} curves

As additional validation data, the calculated C_{rss}–V_{ds} curves compared with TCAD simulation results for the D-MOSFET and the FP-MOSFET, respectively, are shown in Fig. 5-5(a) and (b). Each active area was designed for the same R_{ON} of 10 mΩ. In both V_{ds} linear scale (Fig. 5-5(a)) and V_{ds} log scale (Fig. 5-5(b)), the C_{rss} curves of the D-MOSFET corresponded well qualitatively to TCAD results. However, there were relatively large errors with the maximum of 32% at approximately V_{ds} = 0.1 and 10 V. The reason was the same as in the case of C_{oss} modeling, as mentioned in subsection 5.1.1. On the other hand, in the case of the C_{rss} curves of the FP-MOSFET, errors of less than 10% were seen at $V_{ds} \leq 1$ V, and errors of less than 35% were seen at 1 V < $V_{ds} \leq$ 10 V. However, larger errors occurred in the high-V_{ds} region because of the small value of C_{gd}, which is approximately two to three orders of magnitude lower than C_{oss}, as mentioned in subsection 4.3.6.

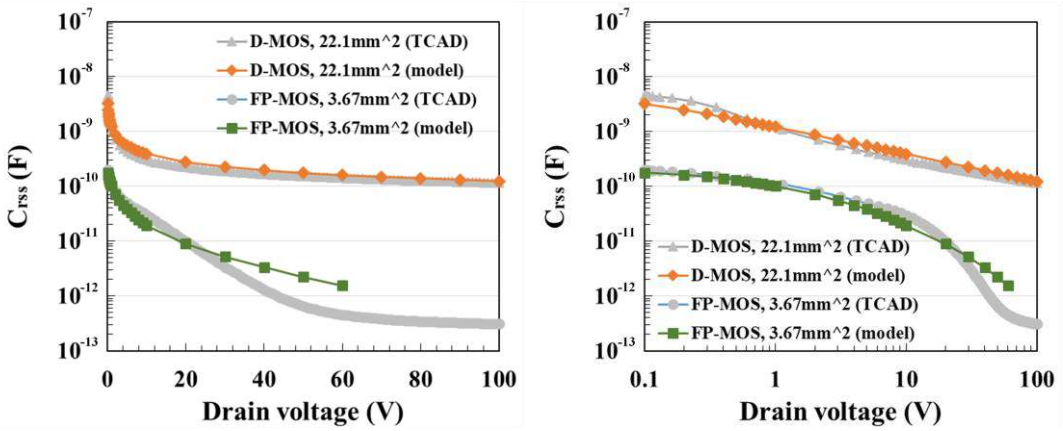


Fig. 5-5. (a) C_{rss}–V_{ds} curves calculated using proposed model compared with TCAD results for 100-V-class D-MOSFET and FP-MOSFET. (a) V_{ds} linear scale and (b) V_{ds} log scale in X-axis. Each active area is designed for the same R_{ON} of 10mΩ. [84] Copyright (2018) The Japan Society of Applied Physics.

5.1.4. Gate–drain charge (Q_{gd})

By using the proposed model, the gate–drain charge Q_{gd} is calculated as

$$Q_{gd} = \int C_{rss}(V_{ds})dV \tag{5-4}$$

Fig. 5-6 show the calculated Q_{gd}–V_{ds} curves compared with TCAD simulation results, for the D-MOSFET and the FP-MOSFET, respectively. Each active area was designed for the same R_{ON} of 10 mΩ. These modeled curves corresponded well qualitatively to TCAD curves. In an application circuit for 100-V-rating device, an input voltage (V_{IN}) of 50 V is assumed generally. In the comparison between the modeled Q_{dg} and the TCAD results at V_{ds} = 50 V, 15 and 11% errors were seen for the FP-MOSFET and the D-MOSFET, respectively. Although these errors are relatively large, it is possible that the calculated results are used for power loss analysis for the FP-MOSFET because the absolute value of the Q_{gd} is approximately one order of magnitude lower than the Q_{oss}.

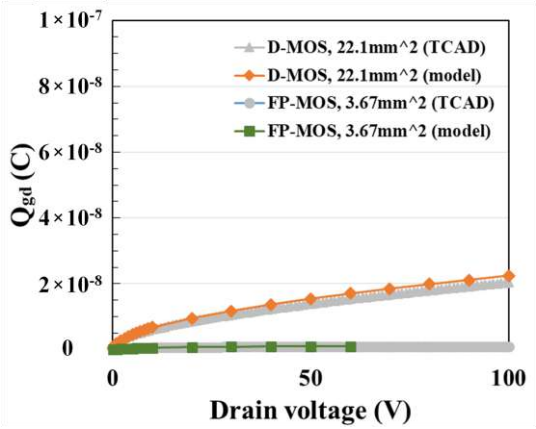


Fig. 5-6. Q_{gd}–V_{ds} curves calculated using proposed model compared with TCAD results for 100-V-class D-MOSFET and FP-MOSFET. Each active area is designed for the same R_{ON} of 10 mΩ.

5.1.5. Switching waveforms

Turn-off switching waveform can be simply calculated using the C_{rss} model. During the turn-off period, the gate voltage V_{gs} is maintained as the mirror voltage, the gate current I_g is constant, and the C_{rss} (C_{gd}) is charged by the I_g. On the other hand, the V_{ds} is varied by dV_{ds}/dt and increases to the input voltage V_{IN}. Thus the I_g is given by

$$I_g = C_{rss}(V_{ds})\frac{dV_{ds}}{dt}. \tag{5-5}$$

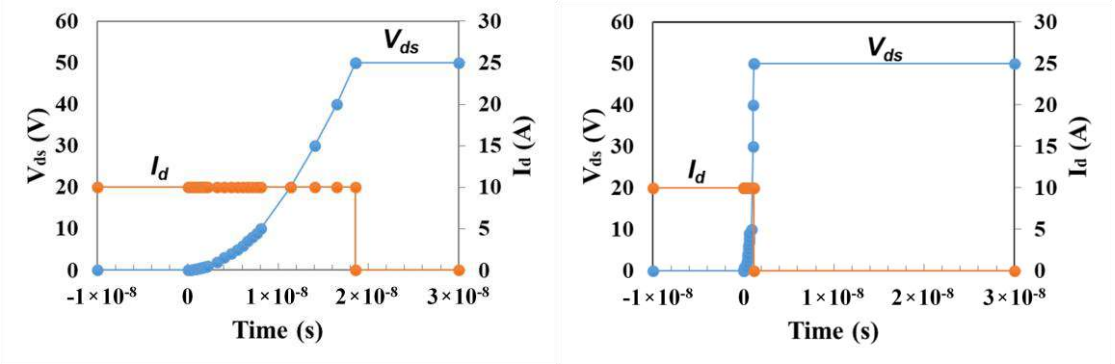
In this period, time t is expressed by using dV_{ds}/dt as below

$$t = \int \frac{dt}{dV_{ds}} dV. \tag{5-6}$$

Therefore, the turn-off time t_{off} is given by

$$t_{off} = \int_0^{V_{IN}} \frac{C_{rss}(V_{ds})}{I_g} dV. \tag{5-7}$$

Fig. 5-7(a) and (b) are the calculated turn-off switching waveforms for the D-MOSFET and the FP-MOSFET, respectively, under the conditions of V_{IN} = 50 V, on-state current I_{ON} = 10 A, gate resistance R_g = 1.5 Ω, and I_g = 0.83 A. As a result, t_{off} = 18.5 ns for the D-MOSFET and t_{off} = 1.1 ns for the FP-MOSFET were calculated using the proposed model. In the calculation, gate–source charge (Q_{gs}), circuit resistance (R_c), and stray inductance (L_s) are not considered.



(a) (b)

Fig. 5-7. Turn-off switching waveforms calculated using proposed model for (a) D-MOSFET and (b) FP-MOSFET. V_{IN} = 50 V, I_{ON} = 10 A, R_g = 1.5 Ω, and I_g = 0.83 A. [84]

5.1.6. Application to other FP-MOSFET structures

As mentioned above, the proposed model for the slant FP-MOSFET was validated. In the case of the conventional flat FP-MOSFET structure, which has a nearly uniform field-plate oxide thickness, the model may be applied. In particular, the results of calculation of Eqs. (4-17) and (4-26) change depending on both T_{FPOX_t} and T_{FPOX_b}. In a future work, a wider application range of the proposed model has to be investigated.

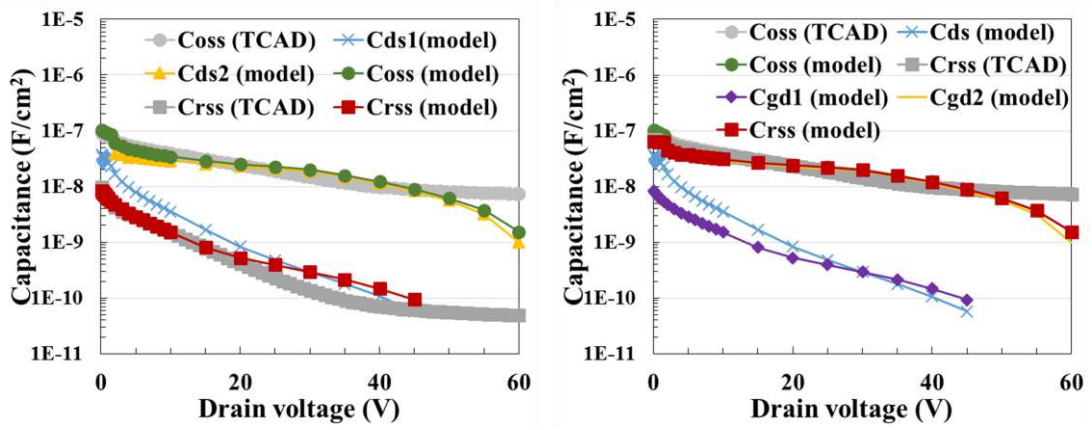
5.2. 60-V-class SFP-MOSFET and GFP-MOSFET

In section 4.4, the comparison of SFP-MOSFET and GFP-MOSFET models were described. The calculated characteristics, using the capacitance model shown in Table 4-10 and the parameters shown in Table 4-8, are validated in the following. [87]

5.2.1. C_{oss}–V_{ds} and C_{rss}–V_{ds} curves

Fig. 5-8(a) and (b) show the C_{oss}–V_{ds} and C_{rss}–V_{ds} curves calculated using proposed model compared with TCAD results, for 60-V-class SFP-MOSFET and GFP-MOSFET. As shown in Table 4-10, there are the following equivalent relations: $C_{ds1}{}^{SFPMOS} = C_{ds}{}^{GFPMOS}$, $C_{ds2}{}^{SFPMOS} = C_{gd2}{}^{GFPMOS}$, $C_{rss}{}^{SFPMOS} = C_{gd1}{}^{GFPMOS}$, and $C_{oss}{}^{SFPMOS} = C_{oss}{}^{GFPMOS}$. Here, C_{ds3} and C_{gd3}, which are trench bottom capacitances, are simply calculated as 0.59 nF/cm^3, however, they are recognized negligible small.

In the C_{oss}–V_{ds} curves, it was confirmed that the calculated results showed good agreement qualitatively to TCAD simulation except for higher voltage region (> 50 V). Numerically, error of 38% were seen at V_{ds} = 30 V. On the other hand, in the C_{rss}–V_{ds} curve of the SFP-MOSFET, errors of less than 5% were seen at $V_{ds} \leq$ 15 V. However, larger errors occurred in the high-V_{ds} region because of the small value of C_{gd}, which is approximately two orders of magnitude lower than C_{oss}, as mentioned in subsection 5.1.1.



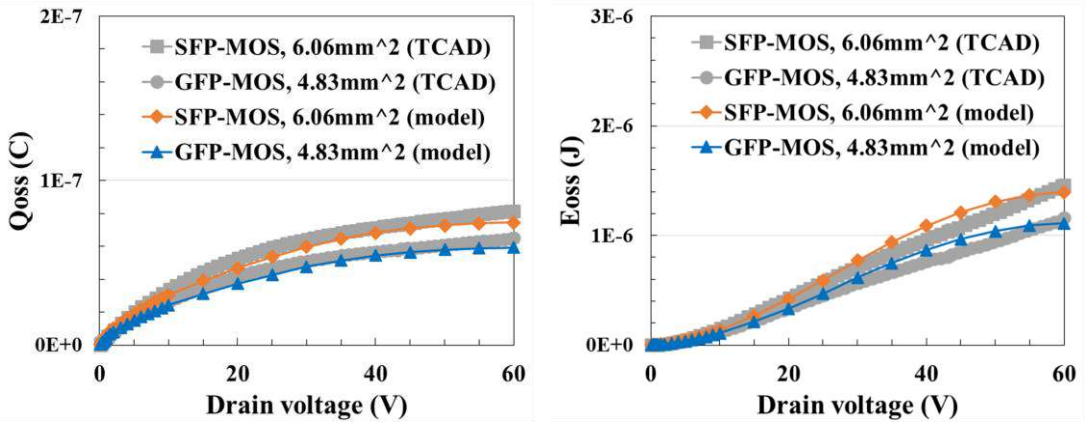
(a) (b)

Fig. 5-8. (a) C_{oss}–V_{ds} and C_{rss}–V_{ds} curves calculated using proposed model compared with TCAD results for 60-V-class SFP-MOSFET. (b) C_{oss}–V_{ds} and C_{rss}–V_{ds} curves calculated using proposed model compared with TCAD results for 60-V-class GFP-MOSFET. [87]

5.2.2. Output charge (Q_{oss}) and stored energy (E_{oss})

To calculate power loss in same condition as described later, an active area of the SFP-MOSFET and the GFP-MOSFET were defined to 6.06 mm² and 4.83 mm², respectively, to achieve same R_{ON} of 1.8 mΩ (cf. Eq. (5-1)). The $R_{ON}A$ of the GFP-MOSFET is 20% lower than that of the SFP-MOSFET as described in subsection 4.4.1, therefore the smaller active area can be realized for the GFP-MOSFET.

Fig. 5-9 (a) and (b) show the calculated Q_{oss}–V_{ds} and E_{oss}–V_{ds} curves (using Eqs. (5-2) and (5-3)) compared with TCAD simulation results, for the SFP-MOSFET and the GFP-MOSFET, respectively. It was obviously that both Q_{oss} and E_{oss} could be lower in the GFP-MOSFET due to the smaller active area. In addition, those values corresponded very well to those of TCAD results. In the SFP-MOSFET, numerically, errors of 7 and 8% were seen at V_{ds} = 30 V for the Q_{oss} and E_{oss}, respectively. Also in the GFP-MOSFET, numerically, errors of 7 and 8% were seen at V_{ds} = 30 V for the Q_{oss} and E_{oss}, respectively.



(a) (b)

Fig. 5-9. (a) Q_{oss}–V_{ds} and (b) E_{oss}–V_{ds} curves calculated using proposed model compared with TCAD results for 60-V-class SFP-MOSFET and GFP-MOSFET. Each active area is designed for the same R_{ON} of 1.8 mΩ. [87]

5.2.3. Gate–drain charge (Q_{gd})

Fig. 5-10 shows the calculated Q_{gd}–V_{ds} curves (using Eq. (5-4)) compared with TCAD simulation results, for the SFP-MOSFET and the GFP-MOSFET, respectively. Each active area was designed for the same R_{ON} of 1.8 mΩ. The calculated curves corresponded well qualitatively to TCAD results. In an application circuit for 60-V-rating device, the input voltage (V_{IN}) of 30 V is assumed generally. In the comparison between the modeled Q_{dg} and the TCAD results at V_{ds} = 30 V, 2.5 and 8.6% errors were seen for the SFP-MOSFET and the GFP-MOSFET, respectively. It is recognized that these results are sufficient to use for power loss analysis for both FP-MOSFETs.

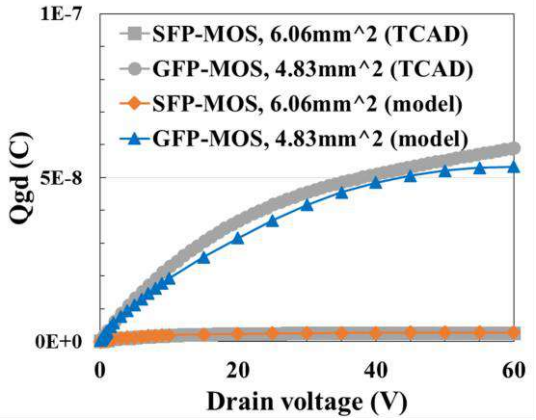
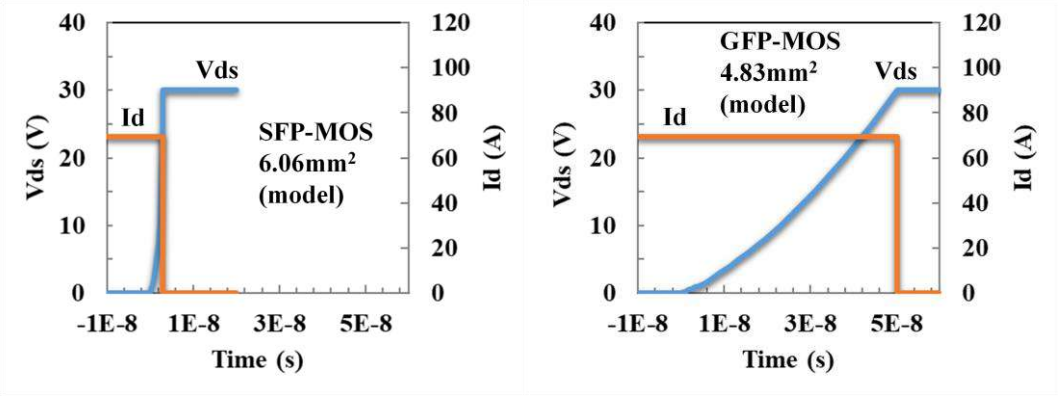


Fig. 5-10. Q_{gd}–V_{ds} curves calculated using proposed model compared with TCAD results for 60-V-class SFP-MOSFET and GFP-MOSFET. Each active area is designed for the same R_{ON} of 1.8 mΩ.

5.2.4. Switching waveforms

Simplified turn-off waveforms could be calculated by using the Crss model. Under the condition of V_{ds}=30 V as the V_{IN} and the drain current I_d = 70 A, the t_{off} in Eq. (5-7) of the SFP-MOSFET was less than one-tenth of that of the GFP-MOSFET, as shown in Fig. 5-11 (a) and (b). High speed turn-off property of the SFP-MOSFET, which is due to the small C_{rss} (Fig. 5-8) and small Q_{gd} (Fig. 5-10), was expressed in the switching waveforms.



(a) (b)

Fig. 5-11. Turn-off switching waveforms calculated using proposed model for (a) SFP-MOSFET and (b) GFP-MOSFET. V_{IN} = 30 V, I_{ON} = 70 A, R_g = 3 Ω, and I_g = 0.83 A. [87]

5.3. Case study for cell pitch shrinking of 100-V-class FP-MOSFET

As other case study, the characteristics regarding the W_{Cell} shrinking of the 100-V-class FP-MOSFET are validated. The capacitance model shown in Table 4-5 and the common parameters shown in Table 4-7 are used in the following calculation.

5.3.1. C_{oss}–V_{ds} curves

In the FP-MOSFET, the W_{Cell} can be shrunk by narrower W_T or narrower W_{Mesa}. Regarding the proposed capacitance model described in sections 4.3 and 4.4, it is necessary to take the parameters of the mesa region into account. Here, the W_{Cell} is shrunk from 3.0 to 2.0 μm by changing the W_{Mesa} from 1.5 to 0.5 μm.

Fig. 5-12 and Fig. 5-13 are W_{Cell} dependences of C_{oss}–V_{ds} curve calculated using proposed model compared with TCAD results for 100-V-class FP-MOSFETs. It is noted that C_{ds3}, which is the trench bottom capacitance, is not calculated in this validation, because C_{oss}–V_{ds} beyond 50 V does not need to the Q_{oss} calculation. In the comparison of those C_{oss}–V_{ds} curves, it can be seen that the TCAD results and the calculated results are good agreement.

5.3.2. C_{oss} and Q_{oss}

Table 5-1 shows TCAD simulated basic characteristics (V_B, $R_{ON}A$, C_{oss} and Q_{oss}) and calculated C_{oss} and Q_{oss} by proposed model for 100-V-class FP-MOSFETs, when the W_{Cell} varies from 3.0 to 2.0 μm. As the accuracy of the model, errors of less than 10% and 8% are confirmed for the C_{oss} and Q_{oss}, respectively. There is not significant problem in the case of the narrow W_{Mesa} calculation, up to 0.5 μm.

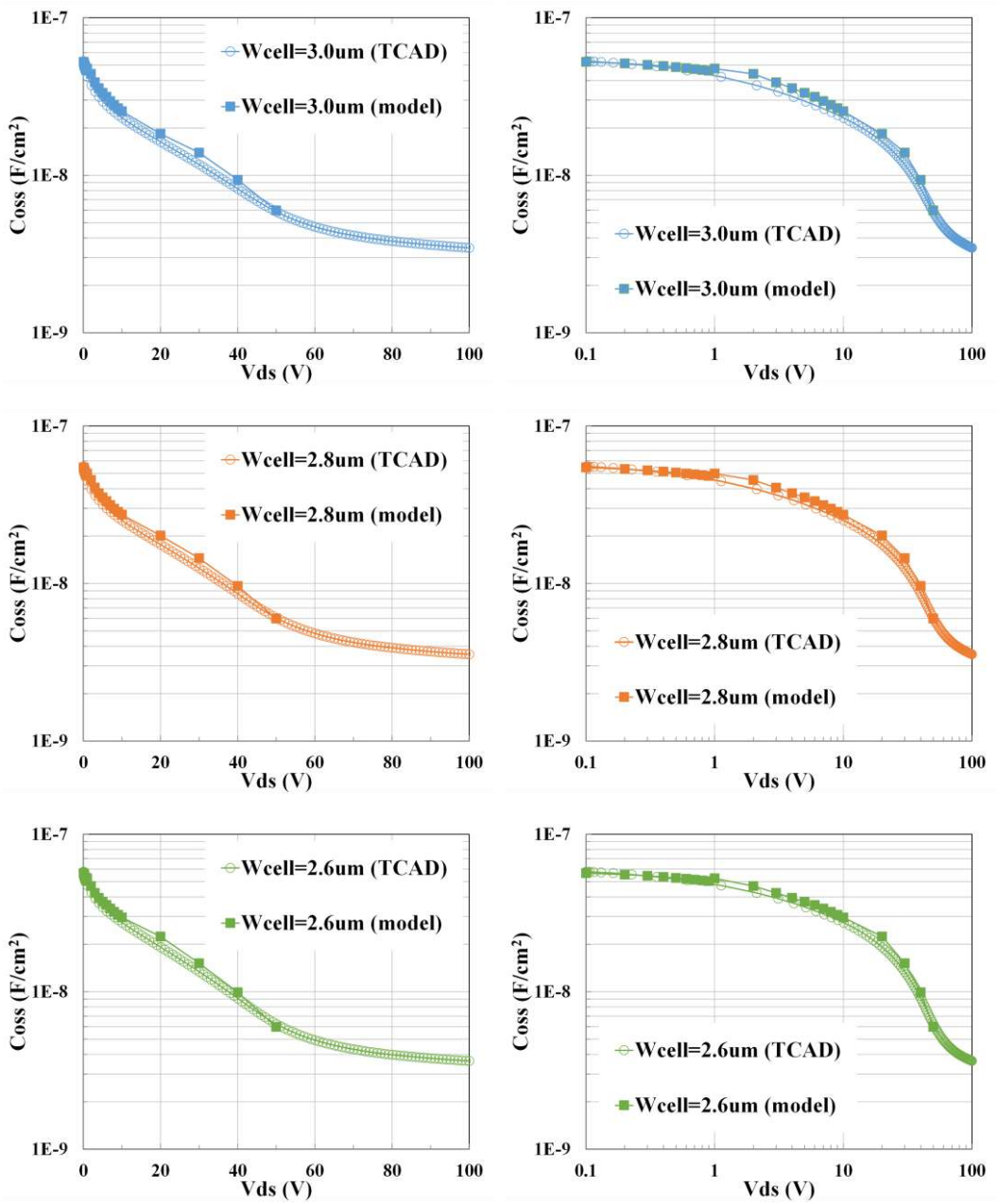


Fig. 5-12. W_{Cell} dependences of C_{oss}–V_{ds} curve calculated using proposed model compared with TCAD results for 100-V-class FP-MOSFETs. W_{Cell} is shrunk from 3.0 to 2.6 μm by changing W_{Mesa} from 1.5 to 1.1 μm. In each row, left figure shows V_{ds} linear scale and right figure shows V_{ds} log scale in X-axis.

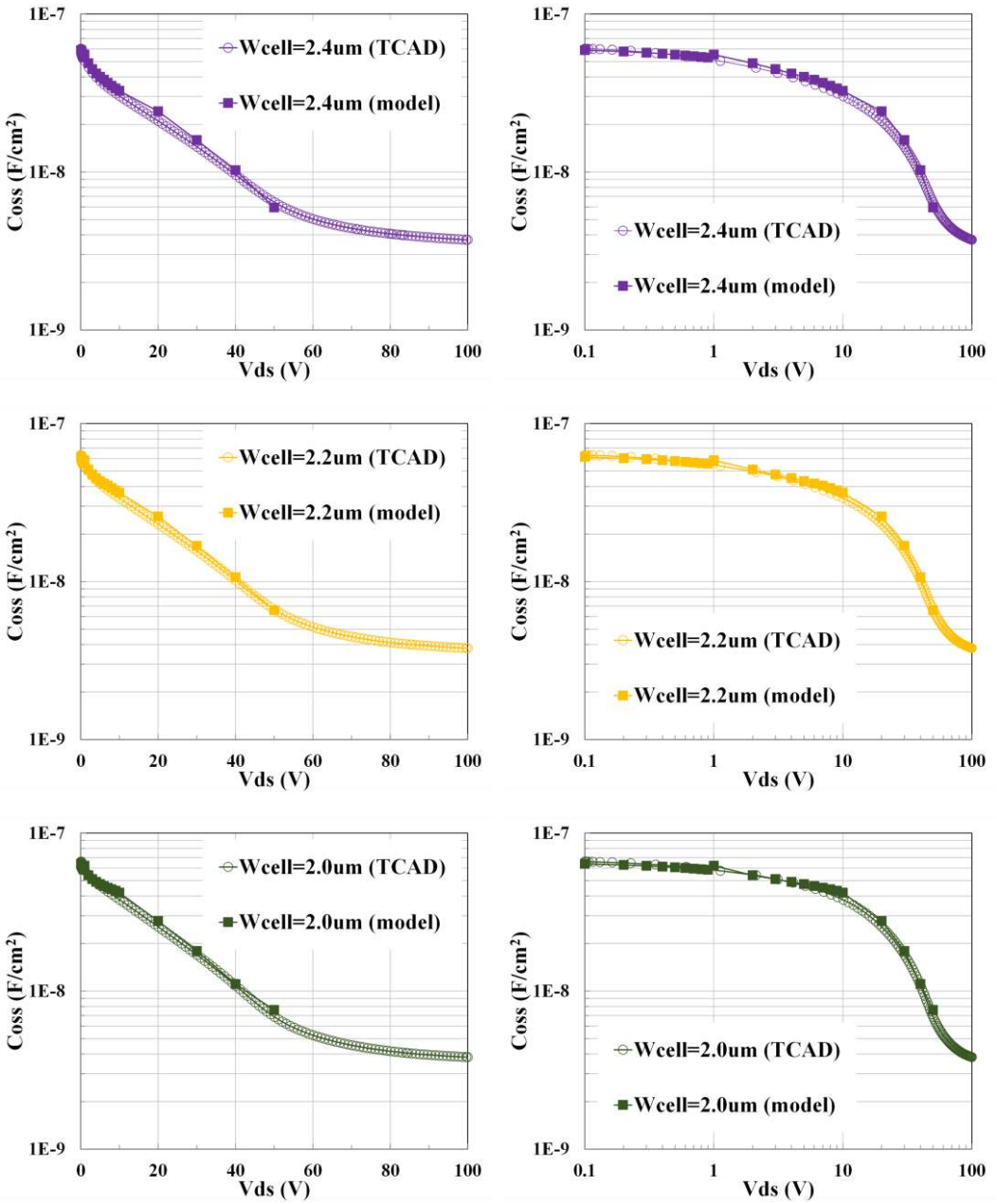


Fig. 5-13. W_{Cell} dependences of C_{oss}–V_{ds} curve calculated using proposed model compared with TCAD results for 100-V-class FP-MOSFETs. W_{Cell} is shrunk from 2.4 to 2.0 μm by changing W_{Mesa} from 0.9 to 0.5 μm. In each row, left figure shows V_{ds} linear scale and right figure shows V_{ds} log scale in X-axis.

Table 5-1. TCAD simulated basic characteristics and calculated C_{oss} and Q_{oss} by proposed model for 100-V-class FP-MOSFETs. Other necessary parameters except W_{Cell}, W_T, W_{Mesa} and N_D are the same as those of Table 4-7.

W_{Cell} (μm)	W_T (μm)	W_{Mesa} (μm)	N_D (atoms/cm^3)	V_B (V)	$R_{ON}A$ (mΩ·mm^2)	C_{oss}/A (pF/mm^2)	Q_{oss}/A (nC/mm^2)	C_{oss}/A (pF/mm^2)	Q_{oss}/A (nC/mm^2)
					V_{gs}=10V	V_{ds}=50V	V_{ds}=50V	V_{ds}=50V	V_{ds}=50V
				TCAD	TCAD	TCAD	TCAD	model	model
3.0	1.5	1.5	2.20×10^{16}	112.9	37.5	58.7	8.14	59.7	8.17
2.8	1.5	1.3	2.54×10^{16}	111.6	35.0	60.6	8.72	59.8	8.62
2.6	1.5	1.1	3.00×10^{16}	110.1	32.8	62.5	9.39	59.7	9.16
2.4	1.5	0.9	3.67×10^{16}	108.2	30.8	64.5	10.2	59.5	9.71
2.2	1.5	0.7	4.71×10^{16}	105.7	29.1	66.6	11.1	65.8	10.4
2.0	1.5	0.5	6.60×10^{16}	102.5	28.2	68.7	12.2	75.9	11.3

5.4. Summary

In chapter 5, the accuracy of the model that derived in chapter 4 was validated. Firstly, drain voltage dependences of C_{oss} and C_{rss}, for 100-V-class D-MOSFET and slant FP-MOSFET, were calculated. Then, 60-V-class GFP-MOSFET and SFP-MOSFET were also calculated. Moreover, the cell-pitch shrinking of the 100-V-class FP-MOSFET were studied. The calculated capacitance curves by the proposed model indicated good agreement with the results of TCAD simulation. In addition, output charge Q_{oss}, stored energy E_{oss}, and turn-off switching time, which are necessary for the switching loss analysis, were calculated from the proposed model and were illustrated.

6. Power Loss Analysis for the Latest FP- MOSFETs

6.1. 100-V-class D-MOSFET and FP-MOSFET [9]

6.1.1. Assuming circuit and power loss components

As a comprehensive evaluation of the proposed model, we estimated the power loss assuming a low-side MOSFET of a buck converter circuit for the D-MOSFET and FP-MOSFET, described in section 5.1 [84]. Each active area was designed for the same R_{ON} of 10 mΩ. The operation conditions were V_{IN} = 50 V, output current I_O = 10 A, duty ratio D = 80%, and switching frequency f_{SW} = 100 kHz to 2 MHz. Here, the calculated conduction loss P_{CON}, turn-off loss $P_{SW(off)}$, and output charge loss P_{Qoss} are given by

$$P_{CON} = {I_O}^2 R_{ON} D, \tag{6-1}$$

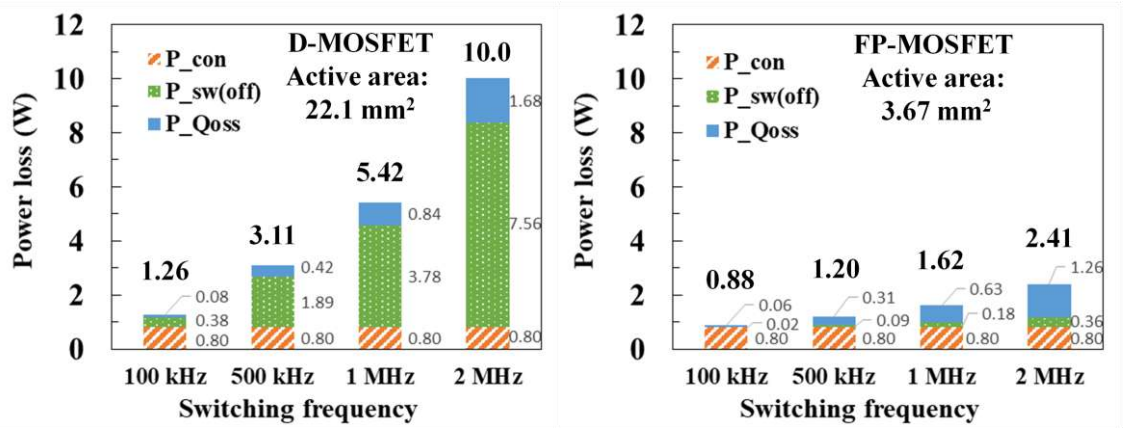
$$P_{SW(off)} = f_{SW} \int_0^{t_{off}} I_O V_{ds} dt, \tag{6-2}$$

$$P_{Qoss} = f_{SW} E_{oss} = f_{SW} \int_0^{V_{IN}} C_{oss}(V_{ds}) V_{ds} dV. \tag{6-3}$$

6.1.2. Power loss estimation by the proposed model

As shown in Fig. 6-1(a) and (b), all P_{CON} values were constant at 0.8 W in both MOSFETs because of the same R_{ON}. $P_{SW(off)}$ was greatly influenced by C_{rss}. Thus, in the D-MOSFET, $P_{SW(off)}$ was the most dominant component and increased to 7.56 W at 2 MHz, because of the large $R_{ON} \cdot C_{rss}$, as shown in Table 4-3. On the other hand, in the FP-MOSFET, the total power loss was drastically suppressed by the low $R_{ON} \cdot C_{rss}$, as shown in Table 4-6, and was mainly increased by P_{Qoss}, which depended on f_{SW}. This analysis reveals that P_{Qoss} may become a significant issue in the case of high-frequency operation, in not only the latest FP-MOSFETs but also next generation FP-MOSFETs.

[9] Section 6.1 is reproduction of [84] section 4.3, Copyright (2018) The Japan Society of Applied Physics, and a part of description is modified.



(a) (b)

Fig. 6-1. Estimated power losses for 100-V-class (a) D-MOSFET and (b) FPMOSFET, assuming 50-V input, 10-A output, 80% duty ratio, and 100 kHz–2 MHz switching operation. Each active area is designed for the same R_{ON} of 10 mΩ. [84] (modified).

6.2. 60-V-class SFP-MOSFET and GFP-MOSFET [10]

6.2.1. Assuming circuit and power loss components

Utilizing the proposed model, main power loss in assumption of an automotive application circuit can be estimated. In the automotive use, there are various specifications of power MOSFETs. For example, 40-V, 60-V and 100-V-rating products are used for 12-V, 24-V and 48-V battery systems. Output current ratings of 5–200 A are needed for various sized motor drive. Though switching frequency (f_{SW}) depends on applied circuit block, 10–100 kHz operation is general. In this subsection, 60-V-class SFP-MOSFET and GFP-MOSFET described in section 5.2 are compared each other [87].

6.2.2. Power loss estimation by the proposed model for high frequency use

In the case of 30-V supply voltage, 50-A load current, and 50% duty ratio, the power loss related to the FP-MOSFET"s features were estimated in various f_{SW} ranged from 20 to 200 kHz, as shown in Fig. 6-2 (a) and (b). The P_{CON} was constant because of same R_{ON} for both devices. In contrary, the $P_{SW(off)}$ which was component of the P_{SW} increased depending on the f_{SW}, especially in the GFP-MOSFET. In the SFP-MOSFET which had very low C_{rss}, total power loss was affected by neither P_{off} nor P_{Qoss} in this frequency

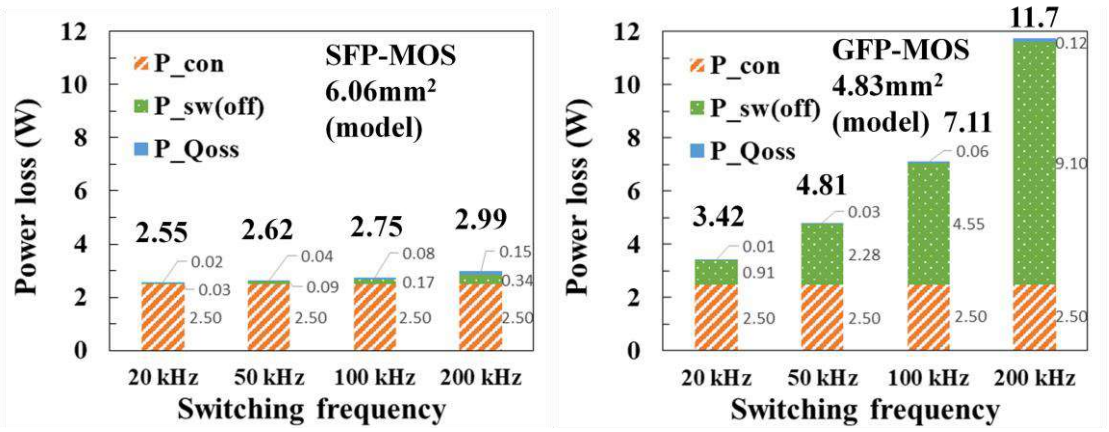


Fig. 6-2. Estimated power losses for 60-V-class (a) SFP-MOSFET and (b) GFP-MOSFET, assuming 30-V input, 50-A output, 50% duty ratio, and 20–200 kHz switching operation. Each active area is designed for the same R_{ON} of 1.8 mΩ.
[87] (modified).

[10] Section 6.2 is reproduction of [87] section 4.2, and a part of description is modified and comprehensive explanations are additionally provided.

range. Therefore, it is obvious that the SFP-MOSFET has great advantage compared with the GFP-MOSFET in the case of 1.8-mΩ class product.

Moreover, the power loss of the f_{SW} ranged from 200 kHz to 2 MHz were estimated for reference. In the GFP-MOSFET shown in Fig. 6-3(b), the $P_{SW(off)}$ increased extremely depending on the frequency, and reached to 95 W in f_{SW} = 2 MHz. On the other hand, in the SFP-MOSFET shown in Fig. 6-3(a), although both $P_{SW(off)}$ and P_{Qoss} increased continuously depending on the frequency, total power loss was suppressed to double of the P_{CON} even in the case of f_{SW} = 2 MHz. It was additionally confirmed that the SFP-MOSFET was appropriate device for mega-hertz-switching application.

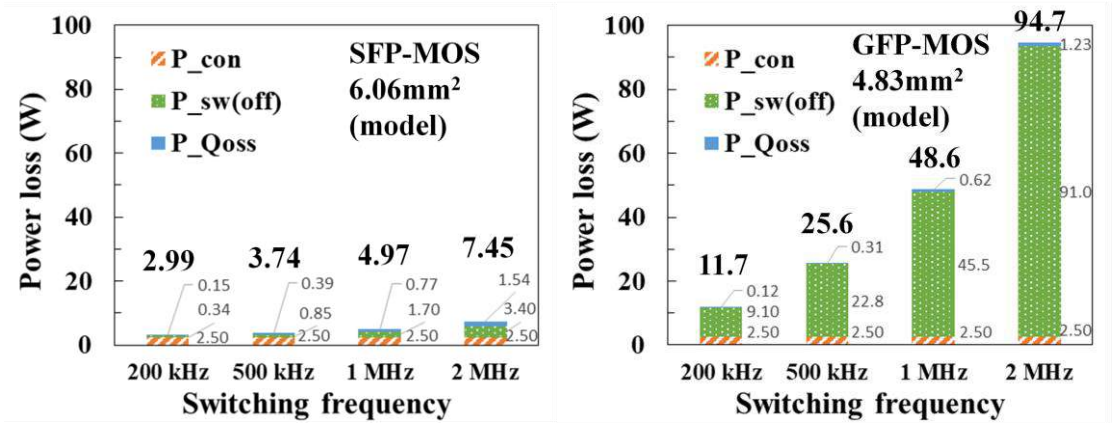


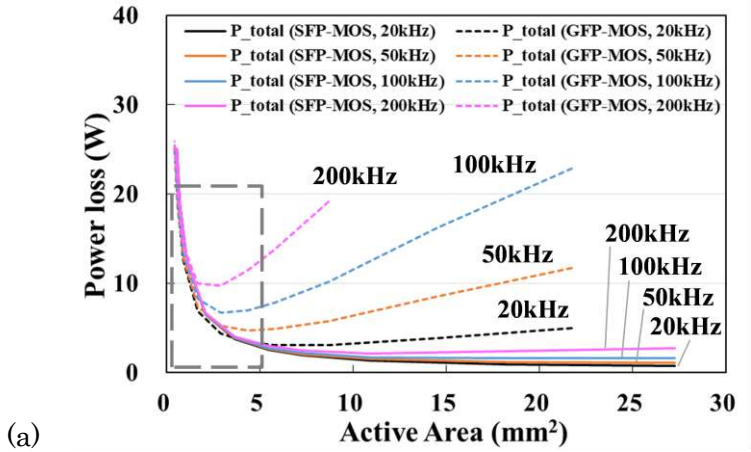
Fig. 6-3. Estimated power losses for 60-V-class (a) SFP-MOSFET and (b) GFP-MOSFET, assuming 30-V input, 50-A output, 50% duty ratio, and 200 kHz–2 MHz switching operation. Each active area is designed for the same R_{ON} of 1.8 mΩ.
[87] (modified).

6.2.3. Power loss estimation by the proposed model for low current use

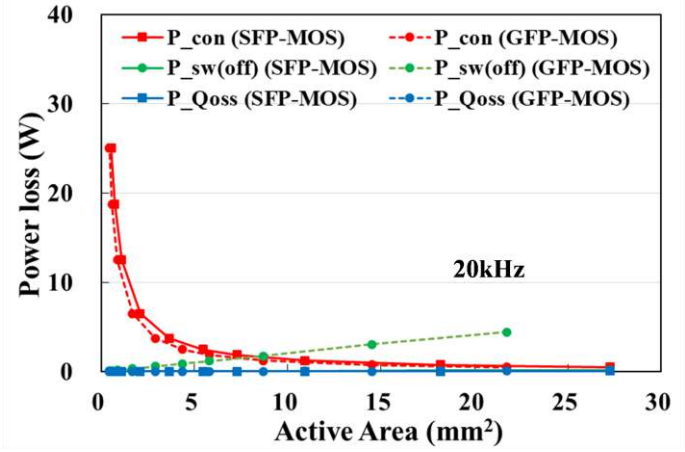
In the case that the f_{SW} is low or the load current is low, which means an application that ultralow R_{ON} is not necessary, the power loss is additionally analyzed.

Fig. 6-4(a) show the active area dependence of the power losses for 60-V-class SFP-MOSFET and GFP-MOSFET in f_{SW} ranged from 20 to 200 kHz. Those were calculated under the condition of 30-V supply voltage, 70-A load current, and 50% duty ratio. Especially in the GFP-MOSFET, the larger the active area, the higher the $P_{SW(off)}$, which could be predicted by Fig. 6-2(b). In the case of smaller active area for both FP-MOSFETs, the total power loss continuously went up due to the P_{CON} increase, which was natural understanding for the higher R_{ON}. That could be also seen in Fig. 6-4(b).

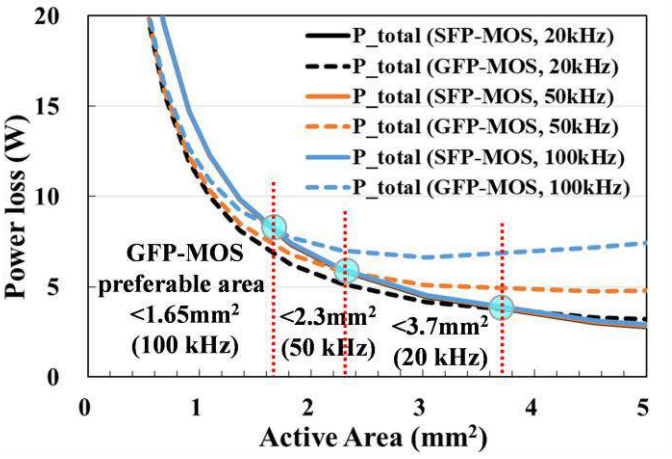
Meanwhile, in a circuit block which does not need ultralow R_{ON}, a power MOSFET product of as low cost as possible is selected in a viewpoint of total system cost. For example, as shown in Fig. 6-4(c), when the f_{SW} was 20 kHz, 3.7-mm^2 active area which corresponds to 2.35 mΩ was boundary for the device selection. Likewise, there would be selectable area under 2.3-mm^2 (corresponds to 3.78 mΩ) in 50 kHz and under 1.65-mm^2 (corresponds to 5.27 mΩ) in 100 kHz. In those case, the GFP-MOSFET, which active area is 20% smaller than that of the SFP-MOSFET, would be preferred (cf. Table 4-9).



(a)



(b)



(c)

Fig. 6-4. (a) Active area dependence of power losses for 60-V-class SFP-MOSFET and GFP-MOSFET in f_{SW} ranged from 20 to 200 kHz, 30-V supply voltage, 70-A load current, and 50% duty ratio. (b) Distinguished to individual losses in 20 kHz. (c) Enlarged view of small active area (< 5 mm²). [87] (modified).

6.3. Summary

In chapter 6, the power loss analysis of the slant FP-MOSFET by the proposed capacitance model was carried out. The power loss calculation that assumed a 100-V-rating device application was performed, and it was confirmed that the performance of the slant FP-MOSFET was superior in high-frequency switching up to 2 MHz.

In addition, the power loss of the 60-V-rating device application was calculated. Source connection field-plate structure (SFP-MOSFET) was effective to a high-current and high-frequency switching use (e.g., 20 kHz–2 MHz). On the other hand, in viewpoint of the device cost, gate connection field-plate structure (GFP-MOSFET) was effective to a low-current use (which means an application that ultralow R_{ON} is not necessary). The active area of the GFP-MOSFET can make 20% reduction compared to that of the SFP-MOSFET, because of the advantage of the small $R_{ON}A$. Moreover, when the application is not high-frequency switching use, the GFP-MOSFET would be very effective as the high-current use.

7. PROPOSAL OF ULTIMATE STRUCTURE FOR HIGH EFFICIENCY POWER MOSFET

As high performance LV-MOSFETs, many R&D achievement for the SJ-UMOSFET and the FP-MOSFET have been reported this decade. It is considered this trend advancing toward so-called "ultimate MOSFET" [88] as low-voltage silicon power device. As one of the approach for the ultimate structure realization, the slant FP-MOSFET that is extremely close to ideal gradient oxide structure was described in section 3.3. Moreover, the structure-based on-resistance models and capacitance models were described in sections 3.3, 4.3, and 4.4.

In this chapter, firstly, a limit of the FP-MOSFET structure is considered. Subsequently, the limitations for structural, electrical, and physical parameters are studied regarding a realistic limit and an ultimate limit. Finally, the performances of both realistic limit and ultimate limit of the FP-MOSFET are predicted.

7.1. Assumptions for ultimate structure proposal of FP-MOSFET

Firstly, as the general power loss in a switching circuit, only conduction loss P_{CON} and output charge loss P_{Qoss} are considered because other power loss components are independent from the drift layer structure. Thus total power loss P_{Loss} is expressed as

$$P_{Total} \approx P_{CON} + P_{Qoss}. \tag{7-1}$$

Secondly, P_{CON} is determined by $R_{\mathrm{ON}}A$, as shown in Eq. (6-1) , therefore, a limit structural parameter to minimize the $R_{\mathrm{ON}}A$ is considered. In the FP-MOSFET structure, $R_{\mathrm{A}}A$ and $R_{\mathrm{SUB}}A$ can be ignored because those are independent from the V_{B} design. Thus a limit $R_{\mathrm{ON}}{}^{\mathrm{FPMOS}}A$ is determined as

$$R_{ON}{}^{FPMOS}\mathrm{A} \approx R_{CH}A + R_{D}A. \tag{7-2}$$

Thirdly, P_{Qoss} is calculated by C_{oss}–V_{ds} characteristic, as shown in Eq. (6-3), therefore, a limit structural parameter to minimize the Q_{oss} (or the E_{oss}) is considered. In the FP-MOSFET structure, C_{gd} can be ignored, because it is independent from the V_{B} design. In addition, C_{ds3} can be also ignored, because trench bottom region is cut in ultimate design. Thus a limit $C_{\mathrm{oss}}{}^{\mathrm{FPMOS}}$ is determined as

$$C_{oss}{}^{FPMOS} \approx C_{ds1} + C_{ds2}. \tag{7-3}$$

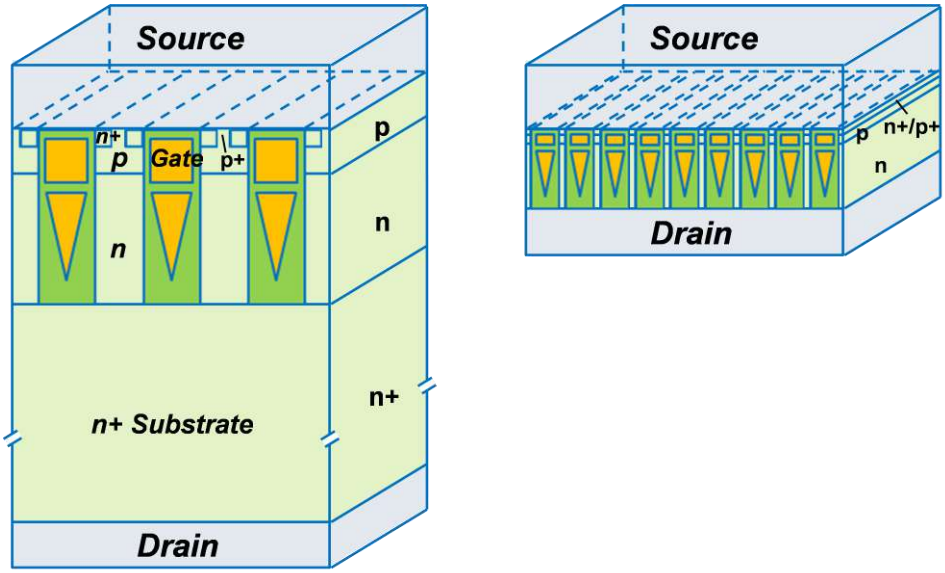
Finally, regarding the V_B, it assumes that an ideal rectangular distribution of the vertical electric field E_y of the drift layer can be achieved (cf. Fig. 3-21(a)). That means field coefficient β is 1 (cf. Eq. (3-40)). Moreover, the buffer layer T_{BUF} is not necessary (cf. Eq. (3-25)). Thus the V_B is obtained as

$$V_B = E_C L_D, \qquad (E_y = E_C). \tag{7-4}$$

In real products, the target V_B is designed to add the rated-voltage of the drain (V_{DSS}). For example, in the case of the V_{DSS} of 100 V, the target V_B is designed to 110 V including 10% margin. In this assumption, the target V_B is decided to 100 V. Actually, the supply voltage is generally restricted to half of the V_{DSS} in the application circuit.

Fig. 7-1(a) and (b) show structure comparison of the latest slant FP-MOSFET and a proposed ultimate FP-MOSFET. The proposed ultimate FP-MOSFET does not has n^+–substrate and has very narrow mesa width. Moreover, each structural parameter is scaled down to limit dimension. Even if the mesa width is extremely narrow, n^+/p^+ interactive pattern has to be on the top of the mesa region in order to maintain the stability of the V_B.

In next section, each parameter limitation is considered.



(a) (b)

Fig. 7-1. Schematic cross sections of (a) the latest slant FP-MOSFET and (b) proposed ultimate FP-MOSFET.

7.2. Consideration of each parameter limitation

7.2.1. MOS channel and p–base region

7.2.1.1. Rated-voltage of gate V_{GSS} and gate oxide thickness T_{GOX}

When the gate oxide thickness T_{GOX} is designed, the rated-voltage of the gate (V_{GSS}) and a gate oxide integrity in the process have to be carefully considered. In mature SiO_2 process, a dielectric breakdown of SiO_2 occurs at an electric-field greater than at least 8 MV/cm, even in the relatively thick oxide film (e.g., 30–50 nm) of the power device [40] [75]. If the necessary V_{GSS} is 20 V, i.e., required for the automobile battery use, the T_{GOX} is designed to 50 nm by the following design concept,

$$T_{GOX} = \frac{2 \times V_{GSS}}{8 \times 10^6 (V/cm)} = 50\ (nm). \tag{7-5}$$

Here, 2× in the denominator means a safe design of the gate oxide to guarantee long term reliability. Actual dielectric breakdown voltage is greater than 40 V under the condition of T_{GOX} = 50 nm. As according to the gate-drive voltage V_{gs} of 5 V that is general logic level of CMOS-IC (complementary MOS integrated circuit), the V_{GSS} is defined to 5 V. In this case, the T_{GOX} in this assumption is decided as below.

$$T_{GOX} = \frac{2 \times V_{GSS}}{8 \times 10^6 (V/cm)} = 12.5\ (nm). \tag{7-6}$$

In this condition of T_{GOX} = 12.5 nm, actual dielectric breakdown voltage is greater than 10 V.

7.2.1.2. Threshold voltage V_{TH} and p–base concentration N_A

When the V_{gs} is fixed as 5 V, the threshold voltage V_{TH} can be lowered from 2.0 to 1.0 V. The V_{TH} is defined by the following.

$$V_{TH} = V_{FB} + \psi_s + \frac{\sqrt{2\varepsilon_{Si}\varepsilon_0 q N_A \psi_s}}{C_{GOX}}, \tag{7-7}$$

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{GOX}}, \tag{7-8}$$

$$\psi_s = \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{7-9}$$

Here, V_{FB} is flat band voltage, ψ_S is surface potential in strong inversion case, φ_{ms} is work function difference, and Q_f is fixed oxide charge. From the text book [89], $\varphi_{ms} = -1.02$ V for n^+–poly-Si on p–Si of $N_A = 5\times10^{17}$ atoms/cm^3 and $Q_f = q\times5\times10^{11}$ C are used for the V_{TH} calculation. By substituting T_{GOX} of 12.5 nm, N_A of 5×10^{17} atoms/cm^3, and the calculated results of Eqs. (7-8)–(7-9) into Eq. (7-7), the V_{TH} is obtained as 0.95 V. It is noted that the N_A has to be increased according to the T_{GOX} thinning, despite of the V_{TH} lowering.

7.2.1.3. Channel length L_{CH}

To investigate a possibility of the channel length L_{CH} shortening, a depletion layer width is calculated in the case of the increased N_A and N_D conditions. The L_{CH} has to be longer than a depletion width of p–base layer side, to prevent the V_B degradation by the punch-though phenomenon.

When the maximum voltage, which equals to the V_{DSS}, applies to drain–source, a depletion layer expands at p–base and n–drift junction. The depletion layer W_{dep_pn} is given by the following,

$$W_{dep\_pn} = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{q}\cdot\left(\frac{N_A + N_D}{N_A N_D}\right)\cdot(V_{bi} + V_{ds})}. \tag{7-10}$$

On the other hand, the depletion layer mainly expands to lightly-doped concentration side that is the n–drift layer. The depletion layer width of the n–drift layer side W_{dep_n} is expressed as,

$$W_{dep\_n} = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{qN_D}\cdot(V_{bi} + V_{ds})}. \tag{7-11}$$

Accordingly, a depletion layer, which expands to the p–base layer side, W_{dep_p} is estimated as the following,

$$W_{dep\_p} = W_{dep\_pn} - W_{dep\_n} \tag{7-12}$$

By substituting N_A of 5×10^{17} atoms/cm^3 and N_D of 4.23×10^{17} atoms/cm^3 into Eqs. (7-10)–(7-12), the W_{dep_p} is obtained as 0.20 μm. Therefore, it can assume that the L_{CH} is

shortened to approximately 0.2 μm. It is noted that the increased N_D will be derived by the following subsection 7.2.2.3.

7.2.2. Field-plate and n–drift region

7.2.2.1. Drift layer length L_D

As mentioned the above, since the target V_B is 100 V, E_C is calculated by Eq. (3-41).

$$E_C = 8.2 \times 10^5 \cdot {V_B}^{-0.2} = 3.26 \times 10^5 \ (V/cm) \tag{7-13}$$

When β is 1, the necessary L_D is calculated by Eqs. (7-4) and (7-13).

$$L_D = \frac{V_B}{E_C} = 3.06 \times 10^{-4} \ (cm) = 3.06 \ (\mu m) \tag{7-14}$$

Here, L_D includes the field-plate length L_{FP}, the bottom thickness of the field-plate oxide T_{FPOX_c}. and the distance between the p–base layer and the upper position of the field-plate.

7.2.2.2. Mesa width W_{Mesa}

To decide a mesa width W_{Mesa} limit, a necessary width in the channel region is considered in the case of the increased N_A conditions. When the interface between the gate oxide and the p–base surface is strong inversion case, a depletion layer W_{d_inv}, which width is greater than the inversion layer width (~10 nm), expands to the p–base surface of the mesa region. W_{d_inv} is given by the following.

$$W_{d\_inv} = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0\psi_s}{qN_A}} = 2\sqrt{\frac{\varepsilon_{Si}\varepsilon_0 kT}{q^2 N_A}\ln\left(\frac{N_A}{n_i}\right)} \tag{7-15}$$

When the N_A is 5×10^{17} atoms/cm^3, the W_{d_inv} is obtained as 0.048 μm (48 nm). Therefore, it can be considered that the W_{Mesa} limit is approximately 0.1 μm.

7.2.2.3. Drift layer concentration N_D

Optimum charge density Q_{Opt} in the mesa region (cf. Eq. (3-43)) is re-calculated by the above E_C.

$$Q_{Opt} = \frac{2E_C\varepsilon_{Si}\varepsilon_0}{q} = 4.23 \times 10^{12}\ (atoms/cm^2). \tag{7-16}$$

Then, when the W_{Mesa} is assumed to 0.1 μm, the N_D is calculated as

$$N_D = \frac{Q_{Opt}}{W_{Mesa}} = \frac{4.15 \times 10^{12}}{1.0 \times 10^{-5}} = 4.23 \times 10^{17}\ (atoms/cm^3). \tag{7-17}$$

7.2.2.4. Electron mobility of n–drift layer μ_{n_D}

It is known that the electron mobility is varied by the doping concentration in silicon. From the text book [86], an electron mobility of n–drift layer μ_{n_D} at room temperature as a function of the N_D is given by the following.

$$\mu_{n\_D} = \frac{5.10 \times 10^{18} + 92{N_D}^{0.91}}{3.75 \times 10^{15} + {N_D}^{0.91}} \tag{7-18}$$

7.2.2.5. Field-plate oxide thickness T_{FPOX}

As the field-plate oxide thickness T_{FPOX} of the 100-V-class FP-MOSFET, 580-nm thick is confirmed to achieve V_B of over 110 V [72], as described in subsection 3.3.3.4. If an insulator of low dielectric constant is adopted instead of the current field-plate oxide (SiO_2), the T_{FPOX} can be thinned. The low dielectric constant insulator is called low-k dielectric film. Here, the dielectric constant of a low-k dielectric film is ε_i.

For example of the low-k material, carbon doped SiO_2 (SiOC), which can be formed by plasma enhanced chemical vapor deposition (PECVD), has been developed to utilize for back end of line (BEOL) process of ultra-large-scale integrated circuit (ULSI) in the 2000s [90] [91] [92] [93]. Objective of the low-k SiOC was to decrease the metal interlayer capacitance of the ULSI in the 90–32 nm technology node, and low-k properties of ε_i = 2.0–2.9 were actually realized. However, it is noted that such a low-k material is restricted to relatively low temperature process, e.g., less than approximately 400 degrees Celsius.

If a material of ε_i = 2.0 is adopted in the FP-MOSFET process, the T_{FPOX} can be thinned as below.

$$T_{FPOX} = 580 \times \frac{\varepsilon_i}{\varepsilon_{OX}} = 297\ (nm). \tag{7-19}$$

Therefore, the T_{FPOX} limit can be designed to 300 nm.

In addition, as an ultimate low-k material, if the field-plate oxide were replaced to an air-gap (ε_i = 1.0) in a future process technology, the T_{FPOX} can be thinned to 150 nm as below.

$$T_{FPOX} = 580 \times \frac{\varepsilon_i}{\varepsilon_{OX}} = 149\ (nm). \tag{7-20}$$

7.3. Prediction of realistic/ultimate limit of FP-MOSFET performance

7.3.1. Structural, electrical, and physical parameters

Based on the consideration of each parameter limitation in section 7.2, necessary parameters to predict both realistic limit and ultimate limit for 100-V-class FP-MOSFET are shown in Table 7-1 and Table 7-2.

Table 7-1. Representative structural parameters of 100-V-class slant FP-MOSFETs to predict realistic limit and ultimate limit.

Symbol	Parameters	Current technology	Realistic limit	Ultimate limit	Unit
W_{Cell}	Cell width	2.60	$W_T + W_{Mesa}$	$W_T + W_{Mesa}$	μm
W_T	Trench width	1.50	$2 \times T_{FPOX\_b}$	$2 \times T_{FPOX\_b}$	μm
W_{Mesa}	Mesa width	1.10	W_{Mesa}	W_{Mesa}	μm
L_{CH}	Channel length	0.30	0.20	0.20	μm
L_A	Accumulation length	0.10	0	0	μm
T_{GOX}	Gate oxide thickness	50	12.5	12.5	nm
N_A	p–Base layer concentration	2.0×10^{17}	5.0×10^{17}	5.0×10^{17}	atoms/cm^3
T_{FPOX_t}	Field-plate oxide thickness (top)	100	100	100	nm
T_{FPOX_b}	Field-plate oxide thickness (bottom)	580	$580 \times \frac{\varepsilon_i}{\varepsilon_{OX}}$	$580 \times \frac{\varepsilon_i}{\varepsilon_{OX}}$	nm
T_{FPOX_c}	Field-plate oxide thickness (center)	580	N/A	N/A	nm
L_{FP}	Field-plate length	4.15	N/A	N/A	μm
L_D	n–Drift layer length	4.93	3.06	3.06	μm
N_D	n–Drift layer concentration	3.0×10^{16}	$\frac{Q_{Opt}}{W_{Mesa}}$	$\frac{Q_{Opt}}{W_{Mesa}}$	atoms/cm^3
Q_{Opt}	Optimum charge of n–drift layer	3.3×10^{12}	4.23×10^{12}	4.23×10^{12}	atoms/cm^2
T_{BUF}	n–Buffer thickness	0.90	0	0	μm
T_{SUB}	n$^+$–Substrate thickness	50	0	0	μm

Table 7-2. Electrical and physical parameters of 100-V-class slant FP-MOSFETs to predict realistic limit and ultimate limit.

Symbol	Parameters	Current technology	Realistic limit	Ultimate limit	Unit
V_{DSS}	Rated-voltage of drain	100	100	100	V
V_B	Target breakdown voltage of drain	110	100	100	V
β	Field coefficient	0.75	1	1	
V_{GSS}	Rated-voltage of gate	20	5	5	V
V_{gs}	Gate-drive voltage	5~12	5	5	V
V_{BD}	Minimum dielectric breakdown voltage	40	10	10	V
V_{TH}	Threshold voltage	2.0	1.0	1.0	V
V_{ON}	On-state voltage	0.10	0.10	0.10	V
μ_{ni}	Electron mobility of inversion layer	500	500	500	cm^2/Vs
μ_{n_D}	Electron mobility of n–drift layer	1096	Depends on N_D	Depends on N_D	cm^2/Vs
ε_{OX}	Dielectric constant of gate oxide (SiO_2)	3.9	3.9	3.9	
ε_i	Dielectric constant of field-plate insulator	3.9	2.0 ~	1.0 ~	

7.3.2. Predicted performances: $R_{ON}A$ and $R_{ON}\cdot Q_{oss}$

As mentioned in section 7.1, $R_{ON}A$ is calculated by sum of $R_{CH}A$ in Eq. (3-27) and R_DA in Eq. (3-30). Because both L_A and T_{BUF} are zero, R_DA is simplified by Eq. (3-32) as below.

$$R_DA = R_{D1}A = \frac{W_{Cell}}{W_{Mesa}}\rho_D L_D \tag{7-21}$$

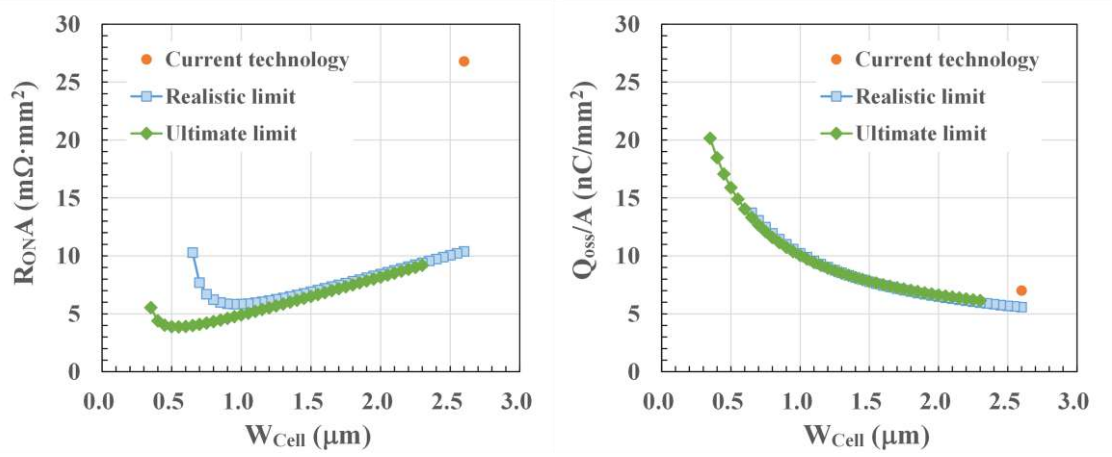
By substituting Eq. (2-12) into Eq. (7-21),

$$R_DA = \frac{L_D}{q\mu_{n\_D}N_D}\frac{W_{Cell}}{W_{Mesa}}. \tag{7-22}$$

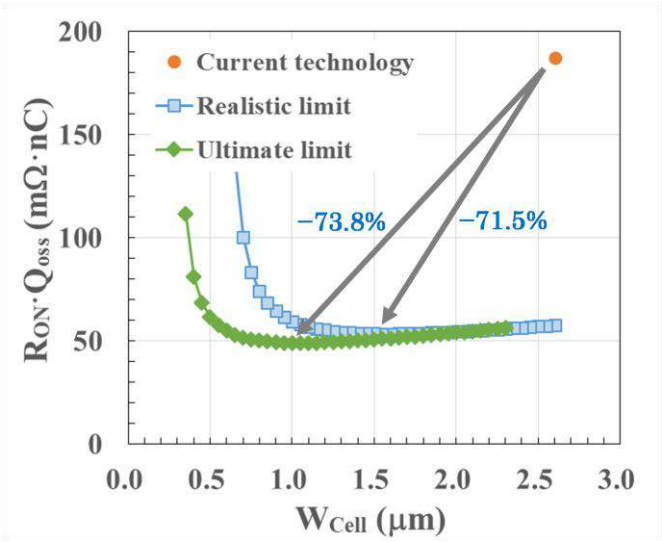
Likewise, as mentioned in section 7.1, C_{oss}/A is calculated by sum of C_{ds1} and C_{ds2} as shown in Table 4-7. Moreover, Q_{oss}/A and E_{oss}/A are derived by Eqs. (5-2) and (5-3).

In the realistic/ultimate limit calculation, W_T is given by $2\times T_{FPOX\_b}$ as shown in Table 7-1. Thus, an optimum W_{Cell} is found out by changing W_{Mesa}. Fig. 7-2 (a)–(c) show the W_{Cell} dependences of $R_{ON}A$, Q_{oss}/A, and $R_{ON}\cdot Q_{oss}$ for realistic limit and ultimate limit prediction of 100-V-class slant FP-MOSFETs. Those prediction is compared with a 2.6-μm-pitch FP-MOSFET, which can be fabricated by current technology (cf. Table 3-7 and Table 4-5). The $R_{ON}A$ reaches minimum at W_{Cell} = 0.95 μm and W_{Cell} = 0.55 μm, for the realistic limit and the ultimate limit, respectively. The Q_{oss} increase monotonically in those W_{Cell} range. Consequently, $R_{ON}\cdot Q_{oss}$, which is one of the FOMs, is minimized at a larger W_{Cell} than that of the $R_{ON}A$. Those are at W_{Cell} = 1.55 μm and W_{Cell} = 1.05 μm for the realistic limit and the ultimate limit, respectively.

Table 7-3 shows calculated $R_{ON}A$, $R_{ON}\cdot Q_{oss}$, and $R_{ON}\cdot E_{oss}$ of 100-V-class slant FP-MOSFETs as realistic limit and ultimate limit. Those results are compared with the current technology. As realistic limit, $R_{ON}A$ and $R_{ON}\cdot Q_{oss}$ are drastically reduced to 5.82 mΩ·mm² and 53.5 mΩ·nC, respectively. Those are 78.2% and 71.5% reduction from those of the current technology. In addition, as ultimate limit, $R_{ON}A$ and $R_{ON}\cdot Q_{oss}$ are drastically reduced to 3.87 mΩ·mm² and 49.1 mΩ·nC, respectively. Those are 85.5% and 73.8% reduction from those of the current technology.



(a) (b)



(c)

Fig. 7-2. W_{Cell} dependences of (a) $R_{ON}A$, (b) Q_{oss}/A, and (c) $R_{ON}\cdot Q_{oss}$ for realistic limit and ultimate limit prediction of 100-V-class slant FP-MOSFETs. These prediction are using structural parameters in Table 7-2 and Table 7-1.

Table 7-3. Calculated $R_{ON}A$, $R_{ON}\cdot Q_{oss}$, and $R_{ON}\cdot E_{oss}$ of 100-V-class slant FP-MOSFETs as realistic limit and ultimate limit. (Bold and underline).

Symbol	Conditions	Current technology	Realistic limit		Ultimate limit		Unit
W_{Cell}		2.6 μm	0.95 μm	1.55 μm	0.55 μm	1.05 μm	
$R_{ON}A$	V_{gs} = 10 V, V_{ON} = 0.1 V	26.7	**<u>5.82</u>**	7.04	**<u>3.87</u>**	5.05	mΩ·mm²
$R_{ON}\cdot Q_{oss}$	V_{ds} = 50 V	187.5	61.7	**<u>53.5</u>**	57.6	**<u>49.1</u>**	mΩ·nC
$R_{ON}\cdot E_{oss}$	V_{ds} = 50 V	3.54	0.93	0.71	0.98	0.71	mΩ·μJ

Fig. 7-3 shows the components of the predicted $R_{ON}A$ of 100-V-class slant FP-MOSFETs, for the realistic/ultimate limit, comparing with those of the current technology. The structural and physical parameters, which minimize each $R_{ON}A$, are adopted as shown in Table 7-4.

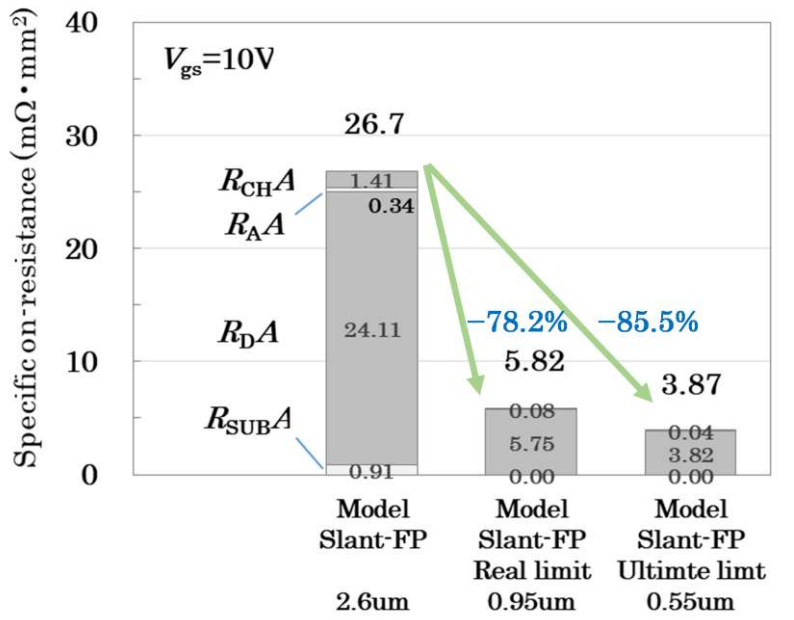
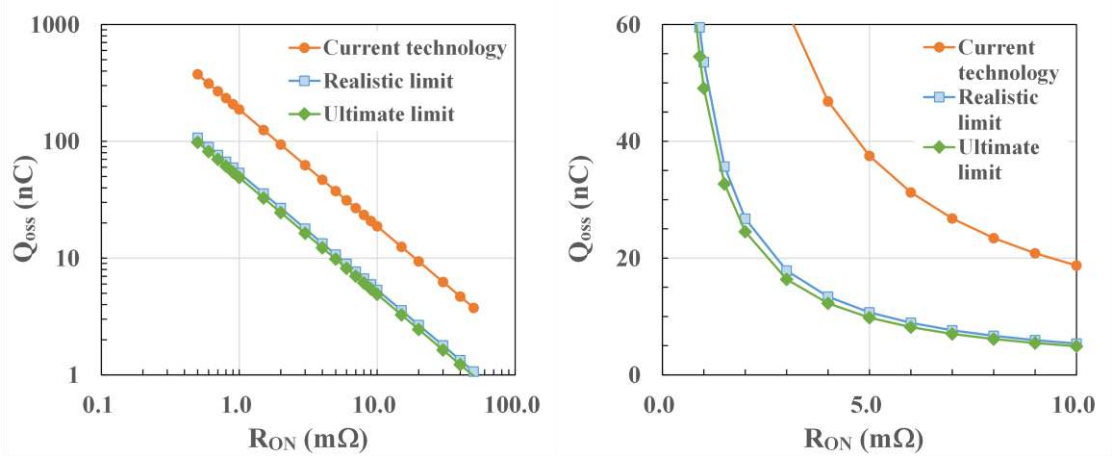


Fig. 7-3. Components of predicted $R_{ON}A$ limit for 100-V-class slant FP-MOSFETs. In comparison of current technology (W_{cell} = 2.6 μm), realistic limit (W_{cell} = 0.95 μm), and ultimate limit (W_{cell} = 0.55 μm). Under the condition of V_{gs} = 10 V.

Table 7-4. Representative structural and physical parameters of 100-V-class slant FP-MOSFETs, which minimize $R_{ON}A$, for realistic limit and ultimate limit.

Symbol	Parameters	Current technology	Realistic limit	Ultimate limit	Unit
W_{Cell}	Cell width	2.60	0.95	0.55	μm
W_T	Trench width	1.50	0.60	0.30	μm
W_{Mesa}	Mesa width	1.10	0.35	0.25	μm
L_{CH}	Channel length	0.30	0.20	0.20	μm
L_A	Accumulation length	0.10	0	0	μm
T_{GOX}	Gate oxide thickness	50	12.5	12.5	nm
N_A	p–Base layer concentration	2.0×10^{17}	5.0×10^{17}	5.0×10^{17}	atoms/cm^3
T_{FPOX_t}	Field-plate oxide thickness (top)	100	100	100	nm
T_{FPOX_b}	Field-plate oxide thickness (bottom)	580	300	150	nm
T_{FPOX_c}	Field-plate oxide thickness (center)	580	N/A	N/A	nm
L_{FP}	Field-plate length	4.15	N/A	N/A	μm
L_D	n–Drift layer length	4.93	3.06	3.06	μm
N_D	n–Drift layer concentration	3.0×10^{16}	1.21×10^{17}	1.69×10^{17}	atoms/cm^3
Q_{Opt}	Optimum charge of n–drift layer	3.3×10^{12}	4.23×10^{12}	4.23×10^{12}	atoms/cm^2
T_{BUF}	n–Buffer thickness	0.90	0	0	μm
T_{SUB}	n$^+$–Substrate thickness	50	0	0	μm
μ_{nD}	Electron mobility of n–drift layer	1096	747	651	cm^2/Vs
ε_i	Dielectric constant of field-plate insulator	3.9	2.0	1.0	

Fig. 7-4(a) and (b) show the tradeoff relationship between R_{ON} and Q_{oss} of 100-V-class slant FP-MOSFETs, in comparison of the current technology, the realistic limit, and the ultimate limit.



(a) (b)

Fig. 7-4. Prediction of tradeoff relationship between R_{ON} and Q_{oss} of 100-V-class slant FP-MOSFETs. (a) Log scale and (b) linear scale in X-/Y-axis.
In comparison of current technology (W_{cell} = 2.6 μm, $R_{ON}\cdot Q_{oss}$ = 187.5 mΩ·nC), realistic limit (W_{cell} = 1.55 μm, $R_{ON}\cdot Q_{oss}$ = 53.5 mΩ·nC), and ultimate limit (W_{cell} = 1.05 μm, $R_{ON}\cdot Q_{oss}$ = 49.1 mΩ·nC).

7.3.3. Predicted performances: Power loss

Utilizing the calculated $R_{ON}A$ and $R_{ON} \cdot Q_{oss}$ of the realistic/ultimate limit for the 100-V-class FP-MOSFET, main power loss (MOSFET power loss) in assumption of a 48-V power supply circuit is additionally predicted. One is a high current automotive application and the other is high switching frequency power supply.

7.3.3.1. Power loss in high current automotive application

In the automotive use, 100-V-rating power MOSFETs are used for 48-V battery systems. High output current over 100 A is required in e.g., an electronic power steering (EPS) or a generator unit. In the case of the three-phase inverter as shown in Fig. 1-8, the circuit consists of six power MOSFETs (three legs × two MOSFETs), which are of same electrical properties. As an assumption for the power loss of one leg, a high-side MOSFET and a low-side MOSFET, which are turned-on/off alternately with duty ratio of 50%, are studied. The switching frequency (f_{SW}) is defined to 100 kHz. As mentioned in section 7.1, only P_{CON} and P_{Qoss} are considered.

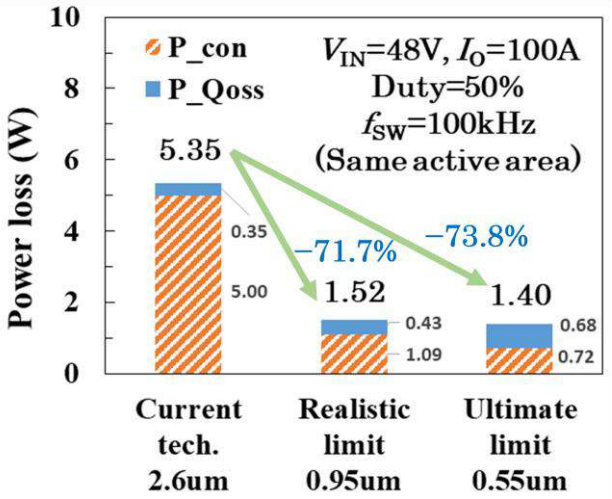


Fig. 7-5. Predicted power loss of 100-V-class FP-MOSFET in high current application. In comparison of current technology (W_{cell} = 2.6 μm, $R_{ON}A$ = 26.7 mΩ·mm²), realistic limit (W_{cell} = 0.95 μm, $R_{ON}A$ = 5.82 mΩ·mm²), and ultimate limit (W_{cell} = 0.55 μm, $R_{ON}A$ = 3.87 mΩ·mm²). Assuming 48-V input, 100-A output, 50% duty ratio, and 100 kHz switching operation. Each active area is the same as that of current technology FP-MOSFET.

Results shows in Fig. 7-5. The P_{CON} occupies main loss. It is confirmed that the realistic limit FP-MOSFET can achieve 71.7% reduction and the ultimate limit FP-MOSFET can achieve 73.8% reduction, for individual MOSFET. It is noted that each active area of the FP-MOSFET is the same as that of current technology FP-MOSFET. That is, R_{ON} of 1.0 mΩ with 26.7 mm^2 for the current technology, 0.22 mΩ with 26.7 mm^2 for the realistic limit, and 0.14 mΩ with 26.7 mm^2 for the ultimate limit.

7.3.3.2. Power loss in high switching frequency power supply

In the power converter circuit of the distributed power supply as shown in Fig. 1-7, 48-V input, 12-V output, and high frequency switching up to 1 MHz are assumed. This circuit consists of four power MOSFETs (two legs × two MOSFETs) in primary side. Corresponding to a step-down ratio V_{OUT}/V_{IN}, each duty ratio for the high-side and the low-side MOSFETs is determined. In this assumption, those are 25% and 75%, respectively. As an appropriate output current, 30-A is assumed. As well as the previous subsection, only P_{CON} and P_{Qoss} are considered.

Results shows in Fig. 7-6(a)–(c). In these case, same R_{ON} of 3.33 mΩ is designed for all high-side MOSFETs to obtain the effect of very small Q_{oss}. In addition, same active area of 8.01 mm^2 is designed for all low-side MOSFETs to obtain the effect of ultralow $R_{ON}A$. Therefore, the P_{Qoss} is improved drastically in the high-side and the P_{CON} is improved drastically in the low-side. As a result, it is confirmed that the realistic limit FP-MOSFET can achieve 54.0% reduction and the ultimate limit FP-MOSFET can achieve 50.9% reduction, for sum of the high-side and the low-side MOSFETs.

In the case of the above assumption, it is noted that the realistic limit FP-MOSFET is slightly superior to the ultimate limit FP-MOSFET. This means the realistic limit structure is sufficiently competitive to the ultimate limit structure. Moreover, it is suggesting that the realizable structure can advance the low-voltage FP-MOSFET performance in near future.

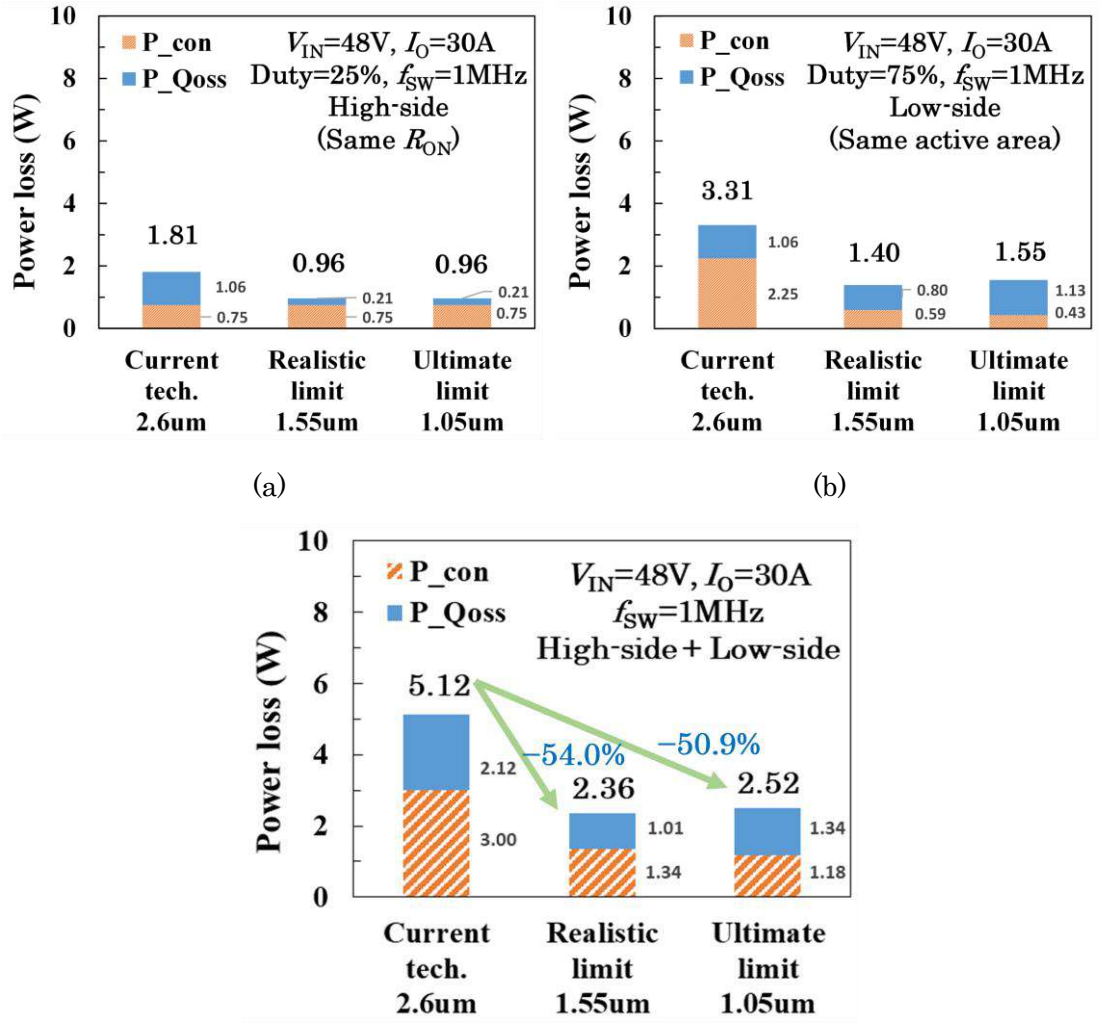


Fig. 7-6. Predicted power losses of 100-V-class FP-MOSFETs in high frequency application, for (a) high-side, (b) low-side, and (c) sum of high-side and low-side. In comparison of current technology (W_{cell} = 2.6 μm), realistic limit (W_{cell} = 1.55 μm), and ultimate limit (W_{cell} = 1.05 μm). Assuming 48-V input, 12-V/30-A output, 1 MHz switching operation, and 25%/75% duty ratio for high-side/low-side. Same R_{ON} of 3.33 mΩ is designed for high-side and same active area of 8.01 mm² is designed for low-side.

7.4. Summary

In chapter 7, by utilizing the $R_{ON}A$ model and the capacitance model of the slant FP-MOSFET, a realistic limit and an ultimate limit of the low-voltage MOSFET performance were considered. The proposed ultimate FP-MOSFET does not has n^+– substrate and has very narrow mesa width. Moreover, each structural parameter is scaled down to limit dimension.

As the realistic limit, $R_{ON}A$ and $R_{ON} \cdot Q_{oss}$ are drastically reduced by 78.2% and 71.5%, respectively, from those of the current technology. In addition, as the ultimate limit, $R_{ON}A$ and $R_{ON} \cdot Q_{oss}$ are more drastically reduced by 85.5% and 73.8%, respectively, from those of the current technology.

In the prediction of power loss for the high current automotive application, the realistic and the ultimate limit FP-MOSFETs can achieve 71.7% and 73.8% reduction, respectively, in the individual MOSFET of the circuit. In the prediction of power loss for the high switching frequency power supply, it is confirmed that the realistic limit FP-MOSFET can achieve 54.0% reduction and the ultimate limit FP-MOSFET can achieve 50.9% reduction, for sum of the high-side and the low-side MOSFETs.

In the assumption, the power loss of the realistic limit is slightly superior to that of the ultimate limit. This means the realistic limit structure is sufficiently competitive to the ultimate limit structure. Moreover, it is suggesting that the realizable structure can advance the FP-MOSFET performance in near future.

8. CONCLUSIONS

The power semiconductor devices are contributing to improve the energy use efficiency in many electronics applications. In particular, silicon power MOSFETs categorized into low-voltage and high-frequency application use are still progressing to meet various market demands. As the device performance that contributes directly to the efficiency, a low-power-loss technology of the power MOSFET is very important. Throughout this research, the plenty of the advanced structures were developed and the superior performances were demonstrated for the low-power-loss MOSFETs. In addition, as important part of this dissertation, the structure-based compact models to enable the power loss calculation in the latest MOSFET structures were newly constructed.

Chapter 1 pointed out that, in addition to the conduction loss improvement by the $R_{ON}A$ reduction, the electric charge accumulated to the output capacitance, which affects to the switching loss, was significant issue particularly in high-frequency switching.

Chapter 2 described the restructured $R_{ON}A$ models of both D-MOSFETs and U-MOSFETs, which were respectively classified into two different patterns: stripe and square cell. The calculated $R_{ON}A$ by the model were compared with the developed devices. In the square cell of the 60-V D-MOSFET, the calculated $R_{ON}A$ corresponded to the experimental result (130 mΩ·mm^2) with only 4.2% error. In the stripe cell of the 30-V U-MOSFET, the calculated $R_{ON}A$ corresponded to the experimental result (5.2 mΩ·mm^2) with less than 1.0% error. Thus it was confirmed those showed good agreement. Meanwhile, in the benchmarking of the tradeoff between the V_B and the $R_{ON}A$ for 20–40-V-class U-MOSFETs, the developed 30-V sub-micron-pitch U-MOSFETs showed superior performance to the published data by approximately 30%.

Chapter 3 described the restructured $R_{ON}A$ models, firstly for the SJ-UMOSFETs, which were classified into three different patterns: stripe, square cell, and square p–column in stripe trench. Then, the models of the FP-MOSFETs were classified into four different structures: flat GFP, flat SFP, slant GFP, and slant SFP. The calculated $R_{ON}A$ by the model were compared with the developed devices. In the square cell of the 60-V SJ-UMOSFET, the calculated $R_{ON}A$ corresponded to the experimental result (28.7 mΩ·mm^2) with only 3.1% error. In the stripe cell of the 100-V FP-MOSFET, the calculated $R_{ON}A$ corresponded to the TCAD simulation (28.2 mΩ·mm^2) with less than 1.0% error. Thus it was also confirmed those showed good agreement. Meanwhile, the benchmarking of the tradeoff between the V_B and the $R_{ON}A$, for 18–100-V-class SJ-UMOSFETs and FP-MOSFETs, were performed. In the developed novel devices, which are the 60-V split p–column SJ-UMOSFET, the 100-V MSO-GFP-MOSFET, the 100-V 2-

step SFP-MOSFET, and the 18-V sub-micron-pitch GFP-MOSFET, each superior performance was demonstrated against the published data.

Chapter 4 described the modeling for the latest slant FP-MOSFET having complex structure, and clarified the components of the parasitic capacitances that are important to the switching loss design of the power MOSFET. The C_{oss} was divided into three elements of C_{ds} and an element of C_{gd} in total. The model equations of both C_{oss} and C_{rss} were constructed based on physical constants and the device structural parameters.

Chapter 5 verified the validity of the constructed models. Firstly, the V_{ds} dependences of C_{oss} and C_{rss}, for both 100-V-class D-MOSFET and slant FP-MOSFET, were calculated. Then, the 60-V-class GFP and SFP-MOSFETs were also calculated. Moreover, the cell-pitch shrinking of the 100-V-class FP-MOSFET was studied. The calculated capacitance curves by the model indicated good agreement with the results of TCAD simulation. In addition, Q_{oss}, E_{oss}, and turn-off switching time, which are necessary for the switching loss analysis, were calculated from the model.

Chapter 6 performed the power loss analysis that assumed the 100-V and 60-V-rating device applications based on the models of $R_{ON}A$ and capacitances. It was revealed that the performance of the slant SFP-MOSFET was superior in high-frequency use (calculation up to 2 MHz), compared with the conventional device. On the other hand, in viewpoint of the system cost, the GFP-MOSFET had advantage for low-current use. The active area of the GFP-MOSFET can make 20% reduction compared to that of the SFP-MOSFET. Moreover, when the application is not high-frequency, the GFP-MOSFET would be effective as high-current use.

Chapter 7 pursued the device performance limit of the slant FP-MOSFET by utilizing the models. In conceivable two case, a realistic limit and an ultimate limit, the device performances were predicted. The $R_{ON}A$ and the $R_{ON} \cdot Q_{oss}$ are drastically reduced by 78.2–85.5% and 71.5–73.8%, respectively, from those of the current technology. As a result, it became clear that the efficiency for the high-frequency switching application can be improved by 50.9–54.0% and that for the low-frequency and high-current application can be improved by 71.7–73.8%. The prediction means the realistic limit structure is sufficiently competitive to the ultimate limit structure.

This dissertation indicated the principle of the future low-power-loss power MOSFET design by utilizing the compact model, which can design in short term without experiment and simulation. Moreover, it revealed that the FP-MOSFET structure has an enough room for the performance improvement and this research area should be advanced more. It is expected this compact model can greatly contribute to higher efficiency power electronics.

Future challenges and perspective are described in the following.

- ✓ Large-scale calculation with this compact model, e.g., by utilizing neural network, would be able to find an optimum solution in very short time. Specifically, e.g., in a circuit including high-side/low-side MOSFETs, plural calculation by structural parameters, load current, switching frequency, duty ratio, etc., is performed at one time. To perform such a demonstration is desirable in the future work.
- ✓ In this research, the components of the power loss were discussed focusing on the MOSFET properties. Even in the case that uses SBD in the converter, the diode recovery loss (P_{Qrr}) does not become zero completely. Modelling of the body-diode or the SBD are one of the important challenges to predict the P_{Qrr} accurately.
- ✓ In the total power loss in the circuit level, voltage over-shoot or current oscillation, which are affected by stray inductances, have to be considered. Coupled analysis by using both semiconductor device and circuit models would become significant more and more.
- ✓ It is recognized that there is a strong demand to expand the compact model to other power devices such as silicon carbide (SiC) or gallium nitride (GaN). The researchers have to face for the challenge.

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REFERENCES

[1] International Energy Agency, "The World Energy Outlook 2017," 2017.

[2] International Energy Agency, "Energy efficiency 2018," 2018.

[3] C. Figueres and M. Philips, "Scaling up demand-side energy efficiency improvements through programmatic CDM," *Energy Sector Management Assistance Program (ESMAP) and The World Bank Carbon Finance Unit,* 2007.

[4] I. Omura, "Semiconductor power switches: principles and the future," *Short course material of the 25th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* 2012.

[5] I. Yoshida, M. Kubo and S. Ochi, "A high power MOSFET with a vertical drain electrode and meshed gate structure," *Technical Digest of International Electron Devices Meeting (IEDM),* pp. 159-162, 1975.

[6] A. Nakagawa, J. Yoshida, T. Utagawa, T. Tsukakoshi, H. Tanabe and T. Kuramoto, "High voltage low on-resistance VDMOS FET," *Proceedings of the 13th Conference on Solid State Devices, 1981; Japanese Journal of Applied Physics, supplement 21-1,* vol. 21, pp. 97-101, 1982.

[7] D. Ueda, H. Takagi and K. G., "A new vertical power MOSFET structure with extremely reduced on-resistance," *IEEE Transactions on Electron Devices,* vol. 32, no. 1, pp. 2-6, 1985.

[8] Y. Baba, N. Matsuda, S. Yanagiya, S. Hiraki and S. Yasuda, "A study on a high blocking voltage UMOS-FET with a double gate structure," *Proceedings of the 4th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 300-303, 1992.

[9] G. Deboy, N. Marz, J.-P. Stengl, H. Strack, J. Tihanyi and H. Weber, "A new generation of high voltage MOSFETs breaks the limit line of silicon," *International Electron Devices Meeting (IEDM) Technical Digest,* pp. 683-685, 1998.

[10] H. Ninomiya, Y. Miura and K. Kobayashi, "Ultra-low on-resistance 60-100 V superjunction UMOSFETs fabricated by multiple ion-implantation," *Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 177-180, 2004.

[11] C. Hu, "A parametric study of power MOSFET's," *Proceedings of IEEE Power Electronics Specialists Conference (PESC),* pp. 385-395, 1979.

[12] R. Sodhi, S. Brown, D. Kinzer, R. Martinez and M. Wiemer, "Integrated design

environment for DC/DC converter FET optimization," *Proceedings of the 11th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 241-244, 1999.

[13] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter and Y. Kawaguchi, "The trench power MOSFET—part II: application specific VDMOS, LDMOS, packaging, and reliability," *IEEE Transactions on Electron Devices,* vol. 64, no. 3, pp. 692-712, 2017.

[14] M. Tsukuda, I. Omura, T. Domon, W. Saito and T. Ogura, "Demonstration of high output power density (30 W/cc) converter using 600 V SiC-SBD and low impedance gate driver," *Proceedings of International Power Electronics Conference (IPEC),* pp. 1184-1189, 2005.

[15] M. Tsukuda, I. Omura, W. Saito and T. Domon, "Demonstration of high output power density (50 W/cc) converter using 600 V SJ-MOSFET and SiC-SBD," *Proceedings of International Conference on Integrated Power Electronics Systems (CIPS 2006),* 2006.

[16] I. Omura, M. Tsukuda, W. Saito and T. Domon, "High power density converter using SiC-SBD," *Proceedings of Power Conversion Conference (PCC),* pp. 575-580, 2007.

[17] A. Schlögl, F. Hirler, J. Ropohl, U. Hiller and M. Rösch, "A new robust power MOSFET family in the voltage range 80 V-150 V with superior low RDSon, excellent switching properties and improved body diode," *European Conf. Power Electronics and Applications,* pp. 1-10, 2005.

[18] J. Roig, D. Lee, F. Bauwens, B. Burra, A. Rinaldi, J. McDonald and B. Desoete, "Suitable operation conditions for different 100V trench-based power MOSFETs in 48V-input synchronous buck converters," *European Conf. Power Electronics and Applications,* 2011.

[19] R. Sodhi, A. Challa, J. Gladish, S. Sapp and C. Rexer, "High cell-density, shielded-gate power MOSFET for improved DC-DC converter efficiency," *Proceedings of PCIM Europe,* pp. 273-, 2010.

[20] W. Choi, D. Son and S. Young, "New power MOSFET technologies optimized for efficient and reliable telecommunication power system," *27th Annual IEEE Applied Power Electronics Conference and Exposition (APEC) ,* pp. 1676-1681, 2012.

[21] T. Sarkar, S. Sapp and A. Challa, "Enhanced shielded-gate trench MOSFETs for high-frequency, high-efficiency computing power supply applications," *28th Annual*

IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 507-511, 2013.

[22] W. Saito, "Comparison of theoretical limits between superjunction and field plate structures," *Proceedings of the 26th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 241-244, 2013.

[23] T. Nishiwaki, T. Hara, K. Kaganoi, M. Yokota, Y. Hokomoto and Y. Kawaguchi, "Design criteria for shoot-through elimination in trench field plate power MOSFET," *Proceedings of the 27th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 382-385, 2014.

[24] Y. Tarui, Y. Hayashi and T. Sekigawa, "Diffusison self-aligned MOST: A new approach for high speed device," *Proceedings of the 1st Conference on Solid State Devices, 1969, Suppliment to Oyo Buturi, the membership Journal of the Japan Society of Applied Physics,* vol. 39, pp. 105-110, 1970.

[25] S. Sun and J. Plummer, "Modeling of the on-resistance of LDMOS, VDMOS, and VMOS power transistors," *IEEE Transactions on Electron Devices,* vol. 27, no. 2, pp. 356-367, 1980.

[26] C. Hu, M.-H. Chi and V. M. Patel, "Optimum design of power MOSFET's," *IEEE Transactions on Electron Devices,* vol. 31, no. 12, pp. 1693-1700, 1984.

[27] K. Shenai, "Optimally scaled low-voltage vertical power MOSFETs for high-frequency power conversion," *IEEE Transactions on Electron Devices,* vol. 37, no. 4, pp. 1141-1153, 1990.

[28] K. Kobayashi, Y. Ninomiya, M. Takahashi and M. Maruoka, "Development of process for low on-resistance vertical power MOSFETs," *NEC Research & Development,* vol. 35, no. 4, pp. 433-437, Oct. 1994.

[29] K. Kobayashi, M. Takahashi, K. Yamaguchi , M. Maruoka, "Development of process for low on-resistance power MOSFETs," *Technical report of IEICE, SDM94-216,* pp. 83-90, 1995.

[30] S. Matsumoto, T. Ohno, H. Ishii and H. Yoshino, "A high-performance self-aligned UMOSFET with a vertical trench contact structure," *IEEE Transactions on Electron Devices,* vol. 41, no. 5, pp. 814-818, 1994.

[31] A. Osawa, Y. Kanematsu, N. Matsuda, T. Yoneda, H. Matsuki, Y. Usui and Y. Baba, "2.5V-driven Nch 3rd generation trench gate MOSFET," *Proceedings of the 11th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 209-212, 1999.

[32] J. Kim, S.-G. Kim, T. M. Roh and B. Lee, "High-density trench DMOSFETs employing two step trench technique and trench contact structure," *Proceedings of the 15th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 165-168, 2003.

[33] A. Narazaki, K. Takano, K. Oku, H. Hamachi and T. Minato, "A marvelous low on-resistance 20V rated self alignment trench MOSFET (SAT-MOS) in a 0.35μm LSI design rule with both high forward blocking voltage yield and large current capability," *Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 393-396, 2004.

[34] K. Kobayashi.U.S. Patent 6888196, May 2005.

[35] D. Ueda, H. Takagi and G. Kano, "An ultra-low on-resistance power MOSFET fabricated by using a fully self-aligned process," *IEEE Transactions on Electron Devices,* vol. 34, no. 4, pp. 926-930, 1987.

[36] H.-R. Chang, R. Black, V. Temple, W. Tantraporn and B. Baliga, "Self-aligned UMOSFET's with a specific on-resistance of 1 mΩ.cm2," *IEEE Transactions on Electron Devices,* vol. 34, no. 11, pp. 2329-2334, 1987.

[37] J. Zeng, G. Dolny, C. Kocon, R. Stokes, N. Kraft, L. Brush, T. Grebs, J. Hao, R. Ridley, J. Benjamin, L. Skurkey, S. Benczkowski, D. Semple, P. Wodarczyk and C. Rexer, "An ultra dense trench-gated power MOSFET technology using a self-aligned process," *Proceedings of the 13th International Symposium on Power Semiconductor Devices & ICs (ISPSD),* pp. 147-150, 2001.

[38] C. Kocon, A. Challa and P. Thorup, "Self-aligned High Density Low Voltage P-Channel Trench MOSFET with Ultra Low Resistance and Robust Ruggedness," *Proceedings of the 18th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 101-104, 2006.

[39] S. Ono, Y. Kawaguchi and A. Nakagawa, "30V new fine trench MOSFET with ultra low on-resistance," *Proceedings of the 15th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 28-31, 2003.

[40] K. Kobayashi, A. Kaneko, Y. Murase and H. Yamamoto, "Sub-micron cell pitch 30 V n-channel UMOSFET with ultra low on-resistance," *Proceedings of the 19th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 205-208, May 2007.

[41] K. Kobayashi, A. Kaneko, Y. Murase , H. Yamamoto, "Sub-micron cell pitch 30V n-channel UMOSFET with ultra low on-resistance," *The papers of joint technical*

meeting on "Electron Devices" and "Semiconductor Power Converter", IEE Japan, EDD-07-77, SPC-07-103, pp. 43-48, Oct. 2007.

[42] K. Kobayashi.U.S. Patent 7429768, 30 Sep. 2008.

[43] S. T. Peake, R. Grover, R. Farr, C. Rogers and G. Petkos, "Fully self-aligned power trench-MOSFET utilizing 1um pitch and 2um trench width," *Proceedings of the 14th International Symposium on Power Semiconductor Devices & ICs (ISPSD),* pp. 29-32, 2002.

[44] M. i. Zandt, E. Hijzen, R. Hueting and G. Koops, "Record-low 4 mohm.mm2 specific on-resistance for 20V trench MOSFETs," *Proceedings of the 15th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 32-35, 2003.

[45] B.-Y. Tsui, T.-C. Gan, M.-D. Wu, H.-H. Chou, Z.-L. Wu and C.-T. Sune, "A novel fully self-aligned process for high cell density trench gate power MOSFETs," *Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 205-208, 2004.

[46] D. Lu, N. Fujishima, A. Sugi, M. Sugimoto, S. Matsunaga, M. Sawada, M. Iwaya and K. Takagiwa, "Integrated bi-directional trench lateral power MOSFETs for one chip lithium-ion battery protection ICs," *Proceedings of the 17th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 355-358, 2005.

[47] B. J. Baliga.U.S. Patent 5637898, Jun. 1997.

[48] B. J. Baliga.U.S. Patent 5998833, Dec. 1999.

[49] G. E. J. Koops, E. A. Hijzen, R. J. E. Hueting and M. A. A. in't Zandt, "Resurf stepped oxide (RSO) MOSFET for 85V having a record-low specific on-resistance," *Proceedings of the 16th International Symposium on Power Semiconductr Devices and ICs (ISPSD),* pp. 185-188, 2004.

[50] M. Kodama, E. Hayashi, Y. Nishibe and T. Uesugi, "Temperature characteristics of a new 100V rated power MOSFET, VLMOS (vertical LOCOS MOS)," *Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 463-466, 2004.

[51] M. A. Gajda, S. W. Hodgskiss, L. A. Mounfield and N. T. Irwin, "Industrialisation of resurf stepped oxide technology for power transistors," *Proceedings of the 18th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 109-112, 2006.

[52] P. Goarin, G. E. J. Koops, R. van Dalen, C. Le Cam and J. Saby, "Splitgate resurf stepped oxide (RSO) MOSFETs for 25 V applications with record low gate-to-drain

charge," *Proceedings of the 19th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 61-64, 2007.

[53] Y. Hattori, K. Nakashima, M. Kuwahara, T. Yoshida, S. Yamauchi and H. Yamaguchi, "Design of a 200V super junction MOSFET with n-buffer regions and its fabrication by trench filling," *Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 189-192, 2004.

[54] S. Yamauchi, T. Shibata, S. Nogami, T. Yamaoka, Y. Hattori and H. Yamaguchi, "200V super junction MOSFET fabricated by high aspect ratio trench filling," *Proceedings of the 18th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 64-48, 2006.

[55] H. Takaya, K. Miyagi, K. Hamada, Y. Okura, N. Tokura and A. Kuroyanagi, "Floating island and thick bottom oxide trench gate MOSFET (FITMOS)," *Proceedings of the 17th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 43-46, 2005.

[56] P. Rutter and S. T. Peake, "Low voltage trenchMOS combining low specific RDS(on) and QG FOM," *Proceedings of the 22nd International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 325-328, 2010.

[57] Y. Kawashima, H. Inomata, K. Murakawa and Y. Miura, "Narrow-pitch n-channel superjucntion UMOSFET for 40-60 V automotive application," *Proceedings of the 22nd International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 329-332, 2010.

[58] J. A. Appels and H. M. J. Vaes, "High voltage thin layer devices (RESURF devices)," *International Electron Devices Meeting (IEDM) Technical Digest,* pp. 238-241, 1979.

[59] J. A. Appels, M. G. Gollet, P. A. H. Hart, H. M. J. Vaes and J. F. C. M. Verhoeven, "Thin layer high-voltage devices (RESURF devices)," *Philips Journal of Research,* vol. 35, no. 1, pp. 1-13, 1980.

[60] T. Fujihira, "Theory of semiconductor super junction devices," *Japanese Journal of Applied Physics,* vol. 36, pp. 6254-6262, 1997.

[61] R. Siemieniec, C. Mößlacher, O. Blank, M. Rösch, M. Frank and M. Hutzler, "A new power MOSFET generation designed for synchronous rectification," *European Conf. Power Electronics and Applications,* pp. 1-10, 2011.

[62] T. Henson and J. Cao, "Low voltage super junction MOSFET simulation and experimentation," *Proceedings of the 15th International Symposium on Power*

Semiconductor Devices and ICs (ISPSD), pp. 37-40, 2003.

[63] S. Yamauchi, Y. Hattori and H. Yamaschi, "Electrical properties of super junction pn diades fabrication by trench filling," *Proceedings of the 15th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 207-210, 2003.

[64] Y. Miura, H. Ninomiya and K. Kobayashi, "High performance superjunction UMOSFETs with split p-columns fabricated by multi-ion-implantations," *Proceedings of the 17th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 39-42, 2005.

[65] Y. Chen, Y. C. Liang and G. S. Samudra, "Theoretical analyses of oxide-bypassed superjunction power metal oxide semiconductor field effect transistor devices," *Japanese Journal of Applied Physics,* vol. 44, no. 2, pp. 847-856, Feb. 2005.

[66] Y. Chen, Y. C. Liang and G. S. Samudra, "Design of gradient oxide-bypassed superjunction power MOSFET devices," *IEEE Transactions on Power Electronics,* vol. 22, no. 4, pp. 1303-1310, Jul. 2007.

[67] Y. Wang, H.-F. Hu, W.-L. Jiao and C. Cheng, "Gate enhanced power UMOSFET with ultralow on-resistance," *IEEE Electron Device Letters,* vol. 31, no. 4, pp. 338-340, Apr. 2010.

[68] Y. Wang, H.-F. Hu and W.-L. Jiao, "High-performance gate-enhanced power UMOSFET with optimized structure," *IEEE Electron Devece Letters,* vol. 31, no. 11, pp. 1281-1283, Nov. 2010.

[69] J. Yedinak, D. Probst, G. Dolny, A. Challa and J. Andrews, "Optimizing oxide charge balanced devices for unclamped inductive switching (UIS)," *Proceedings of the 22nd International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 333-336, 2010.

[70] J. Yedinak, R. Stokes, D. Probst, S. Kim, A. Challa and S. Sapp, "Avalanche instability in oxide charge balanced power MOSFETS," *Proceedings of the 23rd International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 156-159, 2011.

[71] C. Park, S. Havanur, A. Shibib and K. Terrill, "60 V rating split gate trench MOSFETs having best-in-class specific resistance and figure-of-merit," *Proceedings of the 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 387-390, 2016.

[72] K. Kobayashi, T. Nishiguchi, S. Katoh, T. Kawano and Y. Kawaguchi, "100 V class multiple stepped oxide field plate trench MOSFET (MSO-FP-MOSFET) aimed to

ultimate structure realization," *Proceedings of the 27th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 141-144, 2015.

[73] K. Kobayashi, T. Nishiguchi, S. Katoh, T. Kawano and Y. Kawaguchi, "A study of multiple stepped oxide field plate structure for improving a 100 V Class Trench MOSFET," *The papers of joint technical meeting on "Electron Devices" and "Semiconductor Power Converter", IEE Japan, EDD-15-067, SPC-15-149,* pp. 17-22, 2015.

[74] K. Kobayashi, H. Kato, T. Nishiguchi, S. Shimomura, T. Ohno, T. Nishiwaki, K. Aida, K. Ichinoseki, K. Oasa and Y. Kawaguchi, "100-V class two-step-oxide field-plate trench MOSFET to achieve optimum RESURF effect and ultralow on-resistance," *Proceedings of the 31st International Symposium on Power Semiconductor Devices & ICs (ISPSD),* pp. 99-102, 2019.

[75] K. Kobayashi, T. Yamaguchi, S. Tokuda, S. Tsuboi and H. Ninomiya, "An 18V n-channel UMOSFET with super low on-resistance by using vertical resurf structure," *The papers of joint technical meeting on "Electron Devices" and "Semiconductor Power Converter", IEE Japan, EDD-12-068, SPC-12-141,* pp. 49-53, 2012.

[76] H. Takaya, K. Miyagi and K. Hamada, "Advanced floating island and thick bottom oxide trench gate MOSFET (FITMOS) with reduced RonA during AC operation by passive hole gate and improved BVdss RonA trade-off by elliptical floating island," *Proceedings of the 19th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 197-200, 2007.

[77] H. Okubo, K. Kobayashi and Y. Kawashima, "Ultralow on-resistance 30-40 V UMOSFET by 2-D scaling of ion-implanted superjunction structure," *Proceedings of the 25th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 87-90, 2013.

[78] I. Budihardjo and P. Lauritzen, "The lumped-charge power MOSFET model, including parameter extraction," *IEEE Transactions on Power Electronics,* vol. 10, no. 3, pp. 379-387, 1995.

[79] S. Shinohara, "Analysis of power losses in MOSFET synchronous rectifiers by using their design parameters," *Proceedings of the 10th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 347-350, 1998.

[80] R. J. E. Hueting, E. A. Hijzen, A. Heringa, A. W. Ludikhuize and M. A. A. Zandt, "Gate-drain charge analysis for switching in power trench MOSFETs," *IEEE Transactions on Electron Devices,* vol. 51, no. 8, pp. 1323-1330 , 2004.

[81] O. Alatise, N.-A. Parker-Allotey, M. Jennings, P. Mawby, I. Kennedy and G. Petkos, "Modeling the impact of the trench depth on the gate–drain capacitance in power MOSFETs," *IEEE Electron Device Letters,* vol. 32, no. 9, pp. 1269-1271, 2011.

[82] M. Shintani, Y. Nakamura, M. Hiromoto, T. Hikihara and T. Sato, "Measurement and modeling of gate–drain capacitance of silicon carbide vertical double-diffused MOSFET," *Japanese Journal of Applied Physics,* vol. 56, no. 04CR07, 2017.

[83] K. Kobayashi, M. Sudo and I. Omura, "Structure based compact model for output capacitance of trench field-plate MOSFET to enable power loss prediction," *Extended abstracts of the International Conference on Solid State Devices and Materials (SSDM),* pp. 709-710, Sep. 2017.

[84] K. Kobayashi, M. Sudo and I. Omura, "Structure-based capacitance modeling and power loss analysis for the latest high-performance slant field-plate trench MOSFET," *Japanese Journal of Applied Physics,* vol. 57, no. 04FR14, pp. 1-8, Mar. 2018.

[85] Synopsys, Inc., Sentaurus Device User's Manual, 2014.

[86] B. J. Baliga, Fundamentals of Power Semiconductor Devices, New York: Springer, 2008.

[87] K. Kobayashi, M. Sudo and I. Omura, "Power loss analysis of 60 V trench field-plate MOSFETs utilizing structure based capacitance model for automotive application," *Proceedings of the 10th International Conference on Integrated Power Electronics Systems (CIPS),* pp. 122-127, Mar. 2018.

[88] H. Ohashi, "Power devices now and future, strategy of Japan," *Proceedings of the 25th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 9-12, 2012.

[89] S. M. Sze, Semiconductor Devices Physics and Technology 2nd edition, John Wiley & Sons, Inc., 2002.

[90] O. Demolliens, Y. Morand, M. Fayolle, M. Cochet, M. Assous, H. Feldis, D. Lonis, J. Royer, Y. Gobil, G. Passemard, P. Maury, F. Jourdan, M. Cordeau, T. Morel, L. Perroud, L. Ulmer, J. Lugard and D. Renaud, "Copper-SiOC-AirGap integration in a double level metal interconnect," *Proceedings of the International Interconnect Technology Conference,* pp. 276-277, 2000.

[91] S. Lee, T. Yoshie, Y. Sudo, E. Soda, K. Yoneda, B. Yoon, H. Kabayashi, S. Kageyama, K. Misawa, S. Kondo, T. Nasuno, Y. Matsubara, N. Ohashi and N. Kobayashi, "PECVD low-k SiOC (k=2.8) as a cap layer for 200nm pitch Cu interconnect using

porous low-k dielectrics (k=2.3)," *Proceedings of the International Interconnect Technology Conference,* pp. 63-65, 2004.

[92] S. Arakawa, I. Mizuno, Y. Ohoka, K. Nagahata, K. Tabuchi, R. Kanamura and S. Kadomura, "Breakthrough integration of 32nm-node Cu/ultra low-k SiOC (k=2.0) interconnects by using advanced pore-sealing and low-k hard mask technologies," *Proceedings of the International Interconnect Technology Conference,* pp. 210-212, 2006.

[93] N. Asami, T. Owada, S. Akiyama, N. Ohara, Y. Iba, T. Kouno, H. Kudo, S. Takesako, T. Osada, T. Kirimura, H. Watatani, A. Uedono, Y. Nara and M. Kase, "Novel low-k SiOC (k=2.4) with superior tolerance to direct polish and ashing for advanced BEOL integration," *Proceedings of the International Interconnect Technology Conference,* pp. 161-162, 2009.

RESEARCH HISTORY

Publication

1. Kenya Kobayashi, Masaki Sudo and Ichiro Omura, "Structure-based capacitance modeling and power loss analysis for the latest high-performance slant field-plate trench MOSFET," *Japanese Journal of Applied Physics,* vol. 57, no. 04FR14, pp. 1-8, Mar. 2018.

International Conferences

1. Kenya Kobayashi, Masaki Sudo and Ichiro Omura, "Structure based compact model for output capacitance of trench field-plate MOSFET to enable power loss prediction," *Extended abstracts of the International Conference on Solid State Devices and Materials (SSDM),* pp. 709-710, Sep. 2017.
2. Kenya Kobayashi, Masaki Sudo and Ichiro Omura, "Power loss analysis of 60 V trench field-plate MOSFETs utilizing structure based capacitance model for automotive application," *Proceedings of the 10th International Conference on Integrated Power Electronics Systems (CIPS),* pp. 122-127, Mar. 2018.

Related Papers

1. K. Kobayashi, Y. Ninomiya, M. Takahashi and M. Maruoka, "Development of process for low on-resistance vertical power MOSFETs," *NEC Research & Development,* vol. 35, no. 4, pp. 433-437, Oct. 1994.
2. T. Hamajima, K. Kobayashi, H. Kikuchi, K. Okonogi, K. Arai, Y. Ninomiya and M. Takahashi, "Void-free bonded SOI substrates for high voltage, high current vertical DMOS type power ICs," *Japanese Journal of Applied Physics*, vol. 34, part 1, no. 2B, pp. 848-853, 1995.
3. K. Kobayashi, T. Hamajima, H. Kikuchi, M. Takahashi and K. Arai, "An intelligent power device using poly-Si sandwiched wafer bonding technique," *Proceedings of the 7th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pp. 58-62, 1995.
4. K. Kobayashi, T. Hamajima, H. Kikuchi, M. Takahashi and T. Kitano, "Application of partially bonded SOI structure to an intelligent power device having vertical DMOSFET," *Proceedings of the 9th International Symposium on Power*

Semiconductor Devices and ICs (ISPSD), pp. 309-312, 1997.

5. H. Ninomiya, Y. Miura and K. Kobayashi, "Ultra-low on-resistance 60-100 V superjunction UMOSFETs fabricated by multiple ion-implantation," *Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 177-180, 2004.
6. Y. Miura, H. Ninomiya and K. Kobayashi, "High performance superjunction UMOSFETs with split p-columns fabricated by multi-ion-implantations," *Proceedings of the 17th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 39-42, 2005.
7. K. Kobayashi, A. Kaneko, Y. Murase and H. Yamamoto, "Sub-micron cell pitch 30 V n-channel UMOSFET with ultra low on-resistance," *Proceedings of the 19th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 205-208, May 2007.
8. H. Okubo, K. Kobayashi and Y. Kawashima, "Ultralow on-resistance 30-40 V UMOSFET by 2-D scaling of ion-implanted superjunction structure," *Proceedings of the 25th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 87-90, 2013.
9. K. Kobayashi, T. Nishiguchi, S. Katoh, T. Kawano and Y. Kawaguchi, "100 V class multiple stepped oxide field plate trench MOSFET (MSO-FP-MOSFET) aimed to ultimate structure realization," *Proceedings of the 27th International Symposium on Power Semiconductor Devices and ICs (ISPSD),* pp. 141-144, 2015.
10. T. Nishiwaki, S. Katoh, K. Kobayashi and Y. Hokomoto, "Breakdown voltage instability mechanism and improving ruggedness in trench field plate power MOSFET," *Proceedings of the 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pp. 215-218, 2016.
11. T. Nishiwaki, K. Kobayashi and Y. Kawaguchi, "Modeling of time dependent breakdown voltage degradation in trench field plate power MOSFET," *Proceedings of the 29th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pp. 463-466, 2017.
12. H. Kato, K. Kobayashi, T. Nishiguchi, and S. Shimomura, "Process control technique to reduce wafer warpage for trench field plate power MOSFET," *Proceedings of the International Symposium on Semiconductor Manufacturing (ISSM)*, PC-O-26, pp. 1-4, 2018.
13. K. Kobayashi, H. Kato, T. Nishiguchi, S. Shimomura, T. Ohno, T. Nishiwaki, K. Aida, K. Ichinoseki, K. Oasa and Y. Kawaguchi, "100-V class two-step-oxide field-plate trench MOSFET to achieve optimum RESURF effect and ultralow on-resistance,"

Proceedings of the 31st International Symposium on Power Semiconductor Devices & ICs (ISPSD), pp. 99-102, 2019.

14. S. Shimomura, H. Kato. T. Shiraishi, T. Ohno, T. Nishiguchi, K. Miyashita and K. Kobayashi, "Process control technique to dramatically reduce voids in phosphorus-doped poly-silicon for trench field-plate MOSFETs," *Proceedings of the Joint International Symposium on e-Manufacturing & Design Collaboration (eMDC) & Semiconductor Manufacturing (ISSM)*, N5, pp. 1-4, 2019.

Related Patents

United States Patent:

No. 6888196, "Vertical MOSFET produced in cell size and method of producing the same," 2005.

No. 7332770, "Semiconductor device," 2008.

No. 7429768, "Method of manufacturing a semiconductor device having a trench surrounding plural unit cells," 2008.

No. 7508030, "Semiconductor device with vertical MOSFET and method of manufacturing the same," 2009.

No. 7622351, "Method of manufacturing Semiconductor device and Semiconductor device," 2009.

No. 7776693, "Method of manufacturing semiconductor apparatus," 2010.

No. 7893489, "Semiconductor device having vertical MOSFET and method of manufacturing the same," 2011.

No. 8361865, "Method of manufacturing a semiconductor device having vertical MOSFET," 2013.

No. 9525059, "Semiconductor device with graded drift region," 2016.

No. 9536959, "Power semiconductor device having field plate electrode," 2017.

No. 9871131, "Semiconductor device with insulating section of varying thickness," 2017.

No. 9716009, "Semiconductor device with insulating section of varying thickness" 2017.

No. 9947751, "Semiconductor device and method of manufacturing the same," 2018.

No. 9954055, "Vertical power MOSFET device," 2018.

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Kenya Kobayashi was born in Nagano, Japan on February 17, 1969. He received Bachelor degree in electrical engineering from Chiba University, Chiba, Japan, in 1991. He joined NEC Corporation, Kawasaki, Japan, in 1991 and was engaged in the semiconductor devices development, e.g., power MOSFETs, power ICs, high-voltage bipolar ICs, and high-voltage CMOS ICs, for eleven years. He belonged to NEC Electronics Corporation, Kawasaki, Japan, in 2002–2010, and Renesas Electronics Corporation, Kawasaki, Japan, in 2010–2013. He advanced R&D of the power MOSFETs and commercialized many products for eleven years. In October 2013, he moved to Toshiba Corporation, Ishikawa, Japan and he is currently with Advanced Discrete Development Center in Toshiba Electronic Devices & Storage Corporation as a senior manager of the development of power devices process integration technology. He is a holder of 60 U.S. patents, 11 Chinese patents, and 25 Japanese patents.

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