# Development of fast short-circuit protection system for advanced IGBT

M. Ichiki[a], T. Arimoto[a], S. Abe[a], M. Tsukuda[b*], I. Omura[b*]

[a] *Electrical & Electronic Engineering, Graduate School of Engineering, Kyushu Institute of Technology, 1-1 Sensui-cho, Tobata-ku, Kitakyushu-shi, Fukuoka, 804-8550, Japan*

[b] *Department of Biological Functions Engineering, Graduate School of Life Science and Systems Engineering, Kyushu Institute of Technology, 2-4 Hibikino, Wakamatsu-ku, Kitakyushu-shi, Fukuoka, 808-0196, Japan*

**Abstract**

IGBTs, one of the representative power devices, have been increased current density by improving the structure. Even now, new structures have been proposed [1]. It indicates that the current density of IGBTs will continue to increase. To improve conduction characteristics for the higher current density, it is necessary to install a fast short-circuit protection system to prevent the IGBT .

Conventional detection method employs non-isolated current detection such as sense IGBT and shunt resistor. This method detects short-circuit condition after 2us or more because the low-pass filter is embedded to remove noise. In addition, shut-down time is also long by fixed high gate resistance to suppress the surge voltage.

The proposed system consists of a small PCB Rogowski coil, integrator, AD converter, digital circuit (FPGA) and digital gate driver. PCB Rogowski coil detects short-circuit current. The measured current signal is fed to FPGA through ADC. When the digital signal exceeds a threshold considered short-circuit, FPGA outputs shut-down signals to a digital gate driver (Fig. 1).

In short-circuit test with the IGBT rated 1200V/50A connected to a DC voltage source of 600 V, the short-circuit detection time is 70ns (Fig. 2). The shut-down time is reduced by controlling the gate resistance at turn-off.

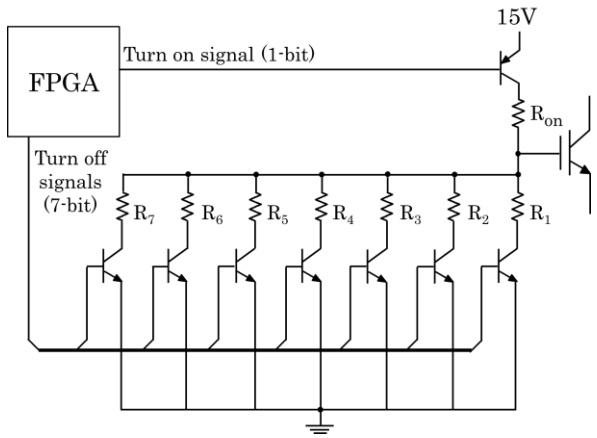


Fig. 1. Diagram of digital gate driver for fast shut-down.

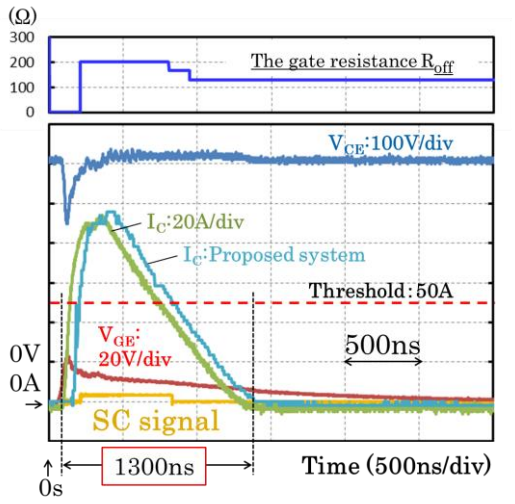


Fig. 2. Short-circuit waveform with proposed system.

**References**

[1] M. Tanaka, I. Omura, "IGBT scaling principle toward CMOS compatible wafer processes", Solid-State Electronics Vol.80, pp.118-123, February 2013.